

# Integration Studies of the Optical Data Link for ATLAS Liquid Argon Calorimeter Readout System

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## Abstract

We present a complete optical data link design for the ATLAS Liquid Argon Calorimeter readout and its integration into the front-end and read out driver systems. The link is based on the G-Link chip configured in a 16-bit double frame mode. A DMILL technology based ASIC multiplexer chip was developed to level shift and 2:1 multiplex the data and to match the G-Link's input requirement. We carried out measurements on the link bit error rate dependence on the frequency, G-Link chip case temperature, and on the G-Link timing characteristics that complement the manufacturer's datasheets.

## I. INTRODUCTION

The G-Link chips (HDMP-1022, HDMP-1024) are widely used in high energy physics experiment data acquisition systems because of the chip's wide reference clock range and its radiation resistance. In the past a conceptual and prototype design of the optical readout system for the ATLAS Liquid Argon calorimeter was presented together with extensive radiation resistance evaluation studies [1,2]. In this report we present a final link design and performance characteristics as well as the studies of the link timing properties and signal characteristics.

The ATLAS Liquid Argon calorimeter front-end board (FEB) output data bus is 32-bit wide, LVDS level with a data rate of 40.08MHz (the LHC clock). In our design the G-Link is configured to be 16-bit input double frame mode. As shown in Figure 1, a DMILL technology based ASIC chip (SMUX) has been developed to level shift and 2:1 multiplex the input 32-bit LVDS data stream to the 16-bit TTL data stream that matches the G-Link input requirement. Radiation resistant optical transmitter module has been developed and radiation resistant fiber has been identified. We also developed an optical receiver module with the ST input connection. Measures were taken to improve this receiver module's sensitivity so that 8 of them can be integrated onto the ROD motherboard.

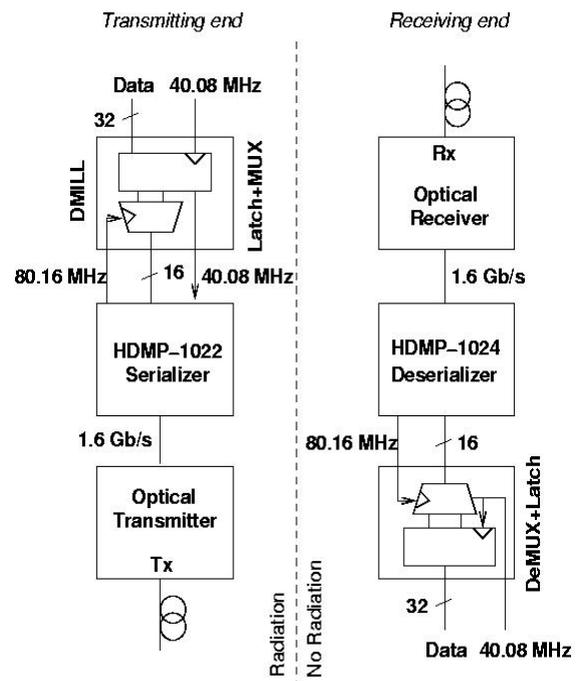


Figure 1: Block diagram of a G-Link based optical data link for the ATLAS Liquid Argon Front End readout.

The multiplexing chip, SMUX, utilizes the STRBOUT signal from the G-Link transmitter chip as its clock reference. In order to understand the STRBOUT duty cycle we constructed an FPGA based G-Link testing board. This board consists of an FPGA based data pattern generator and G-Link transmitter and receiver chips. Optical modules (transmitter and receiver) with a multi-mode graded index fiber are used to connect the G-Link transmitter chip to its receiver chip. The same FPGA chip is also programmed to check the received data and measure the bit error rate. With this testing board the STRBOUT duty cycle is measured to be 62% at 40.08 MHz reference clock, double frame mode.

We operate G-Link in 16-bit input double frame mode with the LHC clock as its reference clock. We use the G-Link testing board to measure the link's maximum baud rate and found it to exceed 1.8 Gbps at room temperature. Since the chip case temperature plays an important roll in the maximum speed, we established an upper limit for operations at 1.8 Gbps baud rate to be 45C.

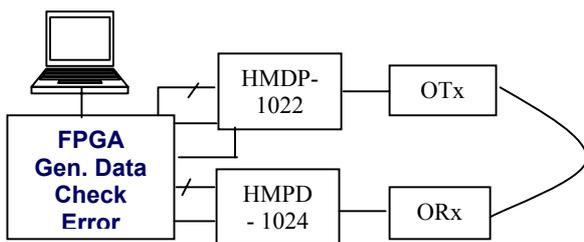
The G-Link transmitter chip samples data with an internal PLL clock based on the input reference clock. The chip also outputs a doubled clock in its STRBOUT signal in double frame mode, to be used in upstream electronics, in our case by a multiplexing chip. We measure the timing relationship between the STRBOUT and the input reference clock, and determined a precise timing window with respect to the STRBOUT when the data are latched and find out that in the 16-bit input double frame mode G-Link starts sampling data at 5.2 ns before the rising edge of the STRBOUT. The sampling window (setup time plus hold time) is measured to be 1.2 ns. This measurement result is valuable for people who use G-Link chips in double frame mode.

We present the above mentioned measurements in detail in the following sections.

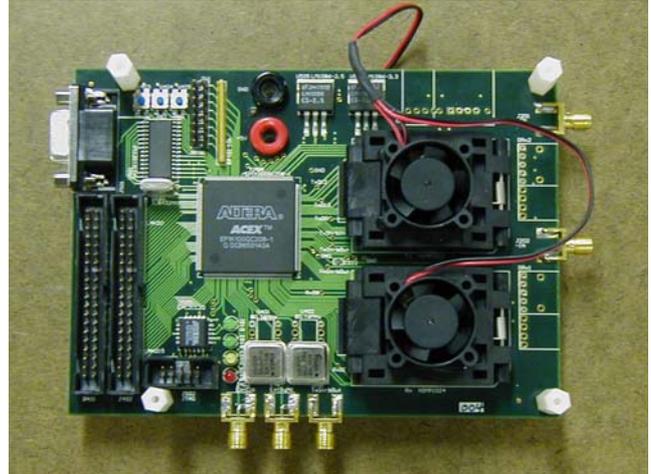
## II. HDMP-1022 STRBOUT DUTY CYCLE

HDMP-1022 provides a STRBOUT signal that the datasheet suggests to be used to clock upstream circuit. In double frame mode, this STRBOUT doubles the input reference clock. We follow the manufacturer datasheet suggestion and use this STRBOUT signal as the clock to our input multiplexer, the DMILL based SMUX. In order to be insensitive to the input 40.08 MHz clock duty cycle, while still maintain a simple ASIC chip design, we use both edges of the STRBOUT signal, so it is essential to know the duty cycle of the STRBOUT. The STRBOUT comes from a PLL clock doubler on the input reference clock. In principle its duty cycle should be 50%. There is no information on the STRBOUT duty cycle in the datasheet after its TTL output driver.

In order to answer this question and many other questions, we designed and constructed a G-Link tester, shown in figure 2.



(a)



(b)

Figure 2: G-Link Tester block diagram (a) and picture of the board (b). The FPGA generates data based on the crystal oscillator. The data with reference input clock are presented to HDMP-1022 that is set to double frame mode. The STRBOUT signal from HDMP-1022 is then measured with a 1.5 GHz bandwidth digital oscilloscope. The PC and the optical modules are not shown in the picture.

A typical measurement is shown below in figure 3. The threshold is set to be 1.4 V and the duty cycle is defined as the width of logical “1” over the period.

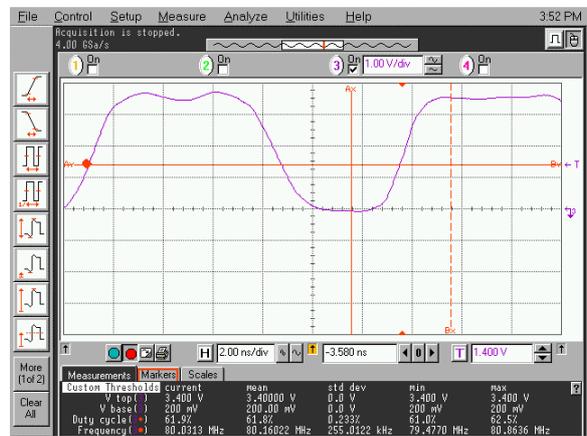


Figure 3: HDMP-1022 STRBOUT waveform.

We measured over 50 chips from different production batches. The result is shown in Figure 4. The average STRBOUT duty cycle is 62.4% with a standard deviation of 0.9%. This deviation of duty cycle from 50% can be explained by the different typical rise and fall times of a TTL driver.

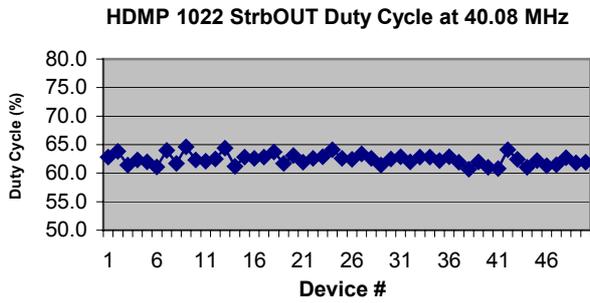
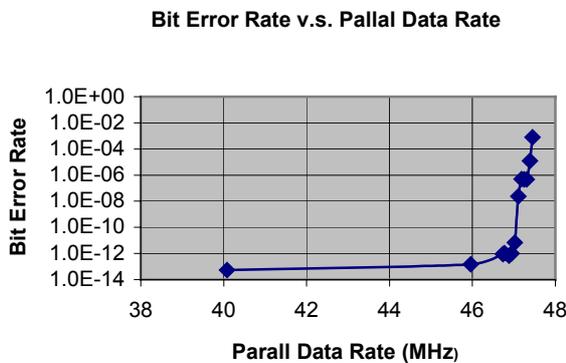


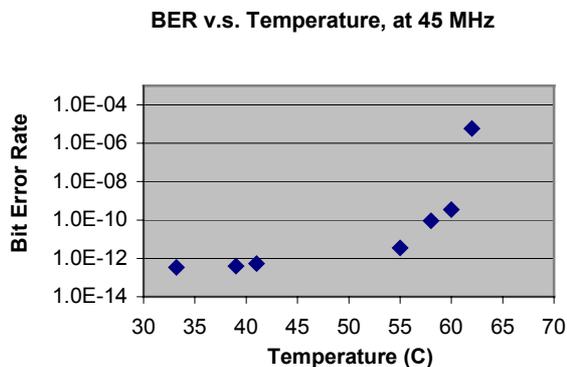
Figure 4: Measurement results of HDMP-1022 STRBOUT duty cycles of 50 chips.

### III. G-LINK OPERATING SPEED AND CASE TEMPERATURE

G-Link is specified to operate at a maximum serial baud rate of 1.5 Gbps [3] with an operation (case) temperature from 0C to 85C. In many applications like in ours, the operation environment is controlled. It is therefore interesting to know the relationship between the operation baud rate and the chip's case temperature. Using our G-Link tester, we scanned the baud rate at room temperature (21C) without forced air flow and the chip case temperature at a baud rate of 1.8 Gbps. The results are shown in figure 5.



(a)



(b)

Figure 5: frequency and temperature scan of the G-Link system. It is clear that at room temperature, with a G-Link case temperature of about 50C, the baud rate is above 1.8 Gbps, while fixing the baud rate at 1.8 Gbps, the chips can operate up to a case temperature of 55C. To give some safety margin, we decide a baud rate of 1.8 Gbps at a case temperature of 45C. In controlled environment, this is achievable with air cooling, while in ATLAS we use water cooling to maintain a case temperature below 35C.

This measurement result is confirmed by Agilent. In reference [3] on page 5, there is a graph that shows a maximum baud rate of 1.8 Gbps without a specification of case temperature. A conversation with Agilent technical support people revealed that the maximum baud rate strongly depend on the case temperature and lower case temperatures do allow the chip to be operated at higher speeds.

### IV. HDMP-1022 INPUT DATA TIMING CHARACTERISTICS

Timing is a very important issue in digital circuit design. G-Link datasheet does provide detailed timing diagrams for single and double frame operation modes. We followed the G-Link datasheet timing diagrams on page 10 and 36 to design our multiplexing chip and adjusted the timing to achieve the best timing widow. This is shown in figure 6, the left side.

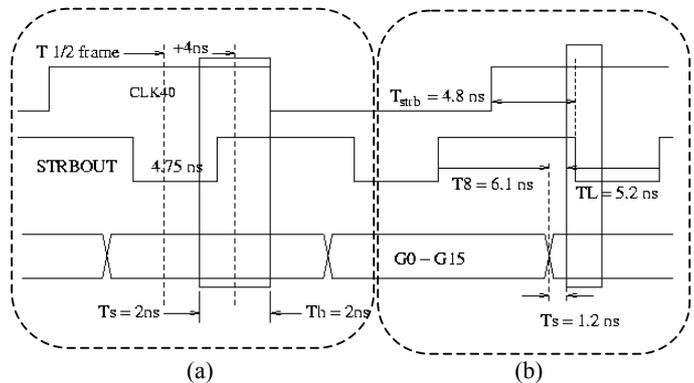


Figure 6: Timing diagram from the G-Link data sheet (a) and from what we measure at the HDMP-1022 input data. According to the G-Link datasheet, we designed a multiplexer that delivers data with perfect timing. According to what we measured, we have a very narrow 1.2 ns timing window.

While checking our system timing margin, we discovered that our system runs only up to 44 MHz parallel input data rate at double frame mode, instead of the measured G-Link speed limit of 45 to 46 MHz. We then realized that there was a timing issue in our system. By moving the phase difference between the data and the input reference clock on our G-Link tester board, we find out that HDMP-1022 actually samples data 5.2 ns before the rising edge of STRBOUT, in double frame mode, instead of 1 ns after this rising edge as stated in the datasheet. Luckily our multiplexing chip is (almost) only clocked by STRBOUT, so fixing this timing problem becomes not very difficult: we added a 10 ns delay line between HDMP-1022 STRBOUT and the multiplexing chip clock input, that effectively moved the data seen by HDMP-1022 2.5 ns earlier in time. Our measurement result is

confirmed through communications with Agilent technical support staff.

## V. CONCLUSIONS

We measured several G-Link's operational characteristics that are either not in its datasheet or incorrect in the datasheet. We believe this information is useful for people who use this G-Link chip in their applications.

## VI. ACKNOWLEDGEMENT

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## VII. REFERENCES

- [1] M.-L. Andrieux et al., Irradiation Studies of Gb/s Optical Links Developed for the Front-end Read-out of the ATLAS Liquid Argon Calorimeter, Nuclear Physics B – Proceedings Supplements 78 (1-3) (1999) pp. 719-724
- [2] M.-L. Andrieux et al., Single-event Upset Studies of a High-speed Digital Optical Data link, Nuclear Instruments and Methods in Physics Research Section A 456 (3) (2001)pp.342-35
- [3] Agilent G-Link datasheet page 5.