Total Ionizing Dose and Single Event Effect Studies of a 0.25µm CMOS Serializer ASIC

Chu Xiang, *Member, IEEE*, Tiankuan Liu, *Member, IEEE*, Cheng-An Yang, Ping Gui, *Member, IEEE,*
Wickham Chen, Junheng Zhang, Peiqing Zhu, Jingbo Ye, *Member, IEEE* and Ryszard Stroynowski

***Abstract*—A 0.25µm CMOS serializer ASIC, designed using radiation tolerant layout practice, was exposed to proton beam at various flux levels and accumulated fluence over 1.9×10^{15} protons/cm^2 (100 Mrad (Si)). The ASIC survived this total ionizing dose (TID) with no degradation in function. Single event effect (SEE) cross-sections are also calculated.**

I. INTRODUCTION

THE Gigabit Optical Link (GOL) is a serial transmitter developed by CERN Microelectronics Group with data rate up to 1.6Gbps [1]. The ASIC chip is implemented in 0.25µm CMOS technology with radiation tolerant layout practices [2]. It is developed for the LHC experiments front-end electronics, and therefore subjected to high doses of ionizing irradiation during the lifetime of the experiments.

System performance of this transmitter ASIC has been tested [3]. Radiation resistance for current LHC applications has been evaluated using X-rays (10 keV peak) in a single step to accumulate total dose of 10 Mrad (SiO_2) at dose rate of 160 rad (SiO_2)/s. Single event upset (SEU) crosstalk was also measured using 60 MeV proton beam with fluence up to 3.14×10^{12} protons/cm^2. No SEU events were observed.

Today, accelerator based high energy physics experiments are conducted at increasingly higher collision rates. The proposed LHC luminosity upgrade will reach 10^{35}/cm^2/sec, 10 times more than current design luminosity. The fluences of secondary particles will also increase by a factor of 10, respectively. Previous studies [4],[5] indicated that the use of radiation tolerant layout practices on deep-submicron CMOS technology, such as enclosed layout, majority voting and up-sizing analog components, extends the tolerable total dose well beyond the inherent technology limit. In the following, we present the results of GOL radiation resistance experiment at the highest reported proton dose and fluence. Section II outlines the design of the GOL chip as well as data analysis system. Experiment setup and irradiation results are described in section III, and section IV concludes the paper.

II. ASIC ARCHITECHURE

The GOL chip deploys basic principles and common architecture of a serializer. It also supports dual-protocol and dual-speed transmission. The configuration registers are accessed via I^{2}C bus and JTAG interface. Serial data output is fed to a 50Ω line driver or a laser driver. Block diagram of the ASIC is shown in Fig. 1. Operation mode stayed the same before, through and after irradiation, as listed in Table I.

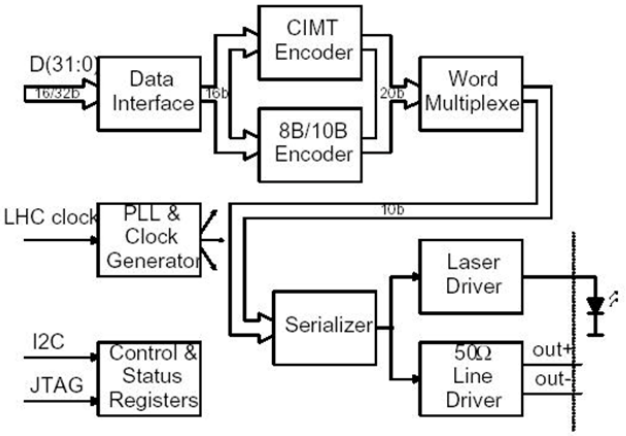

Fig. 1. ASIC architecture of configurable dual-protocol, dual-speed GOL serializer.

TABLE I
ASIC OPERATION MODE CONFIGURATION

Mode	Configuration
coding	8b/10b
word width	32bit
serial data rate	1.6Gbps
PLL wait time	6.55ms
loss of lock tolernace	2 cycles
VCSEL bias	5.8mA
VCSEL modulation	10mA

To evaluate system performance and to carry out online testing during irradiation, we developed a testbed that consists of a complete optical data link and a build-in error rate tester. Schematic drawing of the testbed is shown in Fig. 2. An FPGA mother board generates test patterns and controls, feeds clock and signal to the GOL serializer, detects received data,

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Chu Xiang, Tiankuan Liu, Cheng-An Yang, Jingbo Ye and Ryszard Stroynowski are with Department of Physics, Southern Methodist University, Dallas, TX 75275 USA (telephone: 214-768-1472, e-mail: cxiang@smu.edu).

Ping Gui, Wickham Chen, Junheng Zhang and Peiqing Zhu are with Department of Electrical Engineering, Southern Methodist Univeristy, Dallas, TX 75275 USA (telephone: 214-768-1733, e-mail: pgui@engr. smu.edu).

compares with transmitted data, as well as counts the number of individual bit errors and detected frame errors. Parallel data and control bits are converted into LVDS format to maintain signal integrity between board interfaces. Payload data contains valid 8b/10b encoded frames and intermittent IDLE frames. A Texas Instrument TLK2501 board is used as the receiver. The optical transceivers are a Truelight TTR-1F43-107 VCSEL and a Stratos SLC-25-C-1E SFP.

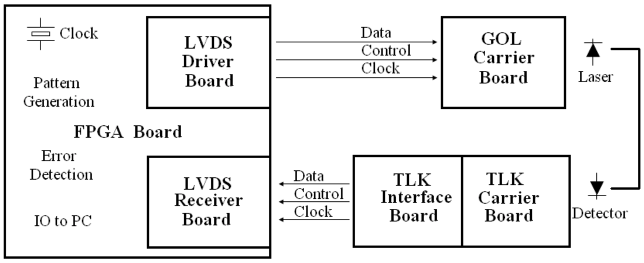

Fig. 2. Block diagram of the test system with complete optical data-link and build-in error rate tester.

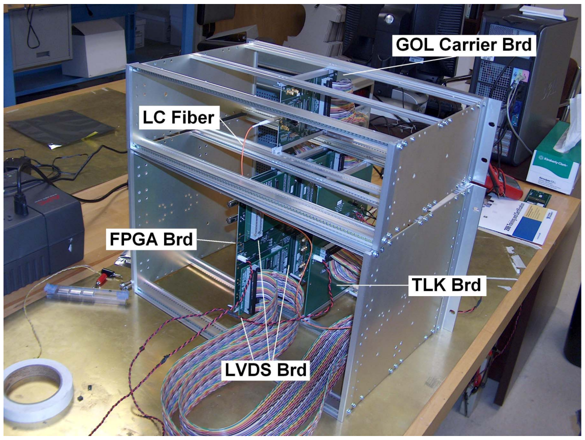

Fig. 3. Picture of the fabricated boards fit into separate VME chaises for in-lab and irradiation test.

The testbed is developed into separate boards to accommodate both system evaluation and irradiation experiment. Only the GOL carrier board is exposed to proton beam while the rest of the system are well shielded from irradiation. These boards fit into two chaises of 3U and 6U VME respectively, as pictured in Fig. 3.

III. RESULTS AND ANALYSIS

Two GOL carrier boards, connected with independent data links and bit error testers, were irradiated at the Massachusetts General Hospital Proton Facility (NPTC) with 230 MeV proton beam. We studied total ionizing dose effect and single event effect in the same experiment. Flux stepped up from 1×10^{7} to 5×10^{11} protons/cm^2/s, and fluence reached 1.9×10^{15} protons/cm^2, corresponding to the total ionization dose of 100 Mrad(Si). The two systems rendered similar results. In the following, we present data from the system that exhibited more irradiation effect.

A. Total ionizing dose results

During beam pauses at scheduled flux steps, and after irradiation reached the planned fluence, data transmissions ran error-free. Both GOL chips withstood a total ionizing dose of 100 Mrad(Si). Currents supplied to GOL chips decreased by less than 4% during the process. Currents consumed by the VCSEL lasers, which were also exposed to proton beam but at reduced density due to their off-center positions, increased 1%. The amount of change in GOL currents did not affect normal chip operation. And the amount of change in VCSEL currents would not cause data transmission error given the margin of optical signal power before irradiation. After two weeks of unbiased, room temperature annealing, the currents returned to their values before irradiation.

Electrical waveforms of serial data were shown in Fig. 4. No changes in rise/fall time were observed, while the amplitude slightly decreased from 350 mV to 300 mV. Both waveforms before and after irradiation comply with modified Gigabit Ethernet standard --- system data rate of 1.6Gbps is determined by the LHC master clock of 40 MHz.

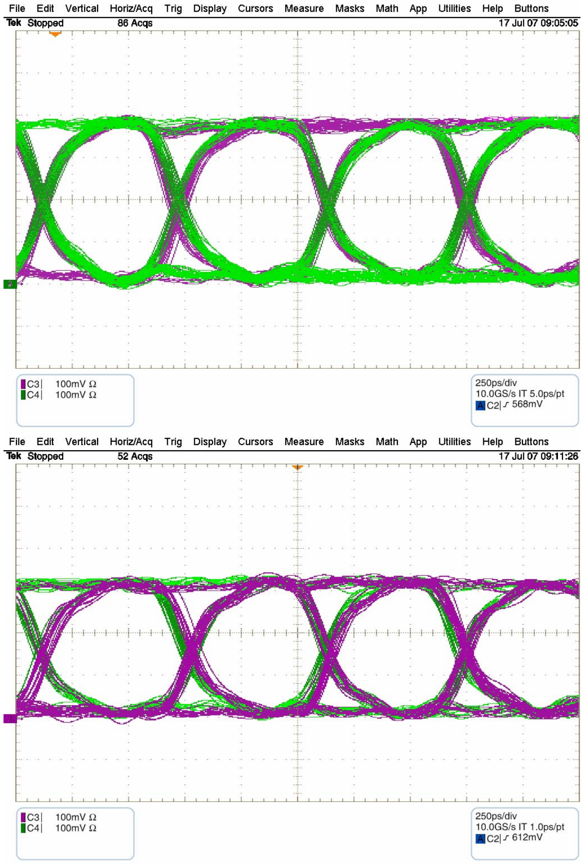

Fig. 4. Serial data waveform (upper: before irradiation; lower: after irradiation with total dose of 100 Mrad(Si)).

Jitter measurements were also performed before and after irradiation to facilitate margin budgeting for application design. GOL jitter generation, which is essentially the integrated phase-noise, was measured as serial output intrinsic jitter in the absence of applied jitter to parallel input. As shown in Table II, change in GOL jitter generation was minimal after irradiation.

TABLE II
TRANSMITTER INTRINSIC JITTER COMPONENTS

	clk	before	after
Random (RMS)	8.6ps	8.8ps	9.9ps
Deterministic (Pk-Pk)	10.8ps	112.5ps	96.6ps
Total @BER	127.7ps	208.6ps	205.2ps

Jitter transfer function of a component is the ratio of the amplitude of output jitter to an applied input jitter [8]. This measurement specifies that no parts of a system will cause an unacceptable increase in jitter and that the recovered signal will follow a tolerance template. We measured transfer function of GOL and of the complete data link by injecting sinusoidal jitter of 200ps at various modulation frequencies up to 1.5MHz to the parallel input of GOL. Results are shown in Fig. 5.

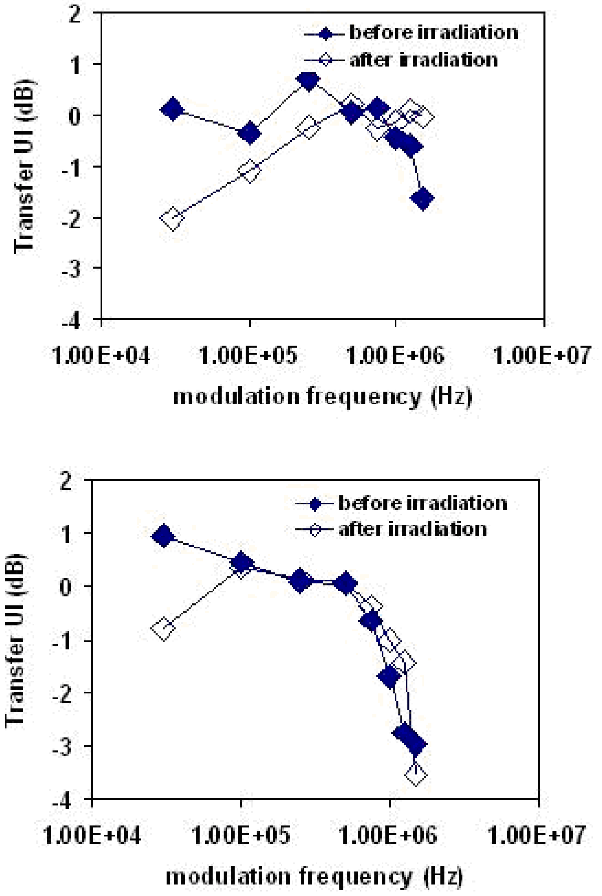

Fig. 5. Jitter transfer function (upper: GOL jitter transfer before and after irradiation; lower: system jitter transfer before and after irradiation).

Flattening of the GOL jitter transfer at high modulation frequency after irradiation indicates that the transmitter's multiplexer bandwidth might have increased. This requires strict control on input signal jitter spectrum. However, there is little change in the overall system jitter transfer after irradiation, showing that the receiver is able to tolerate the above specified injected jitter with GOL transfer function degraded after irradiation.

Jitter tolerance of the complete data link was also tested before and after irradiation. We measured the jitter penalty of equivalence to 1dB power degradation while maintaining better than 1×10^{-12} bit error ratio. As shown in Fig. 6, the applied sinusoidal jitter magnitude and frequency that caused the specified degradation follows SONET/SDH OC48 template well. Irradiation caused no effect on the overall margin.

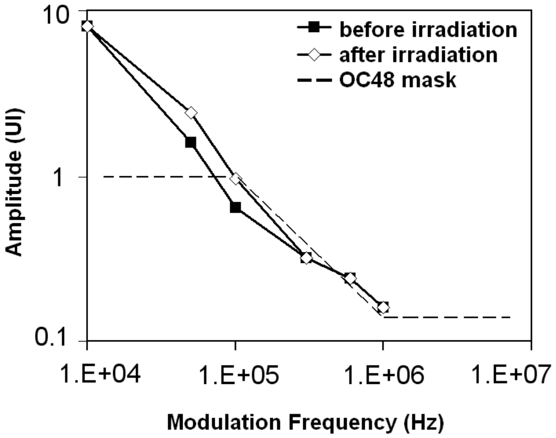

Fig. 6. Jitter tolerance before and after irradiation.

B. Single event effect results

In Table III we summarize the step raised flux levels, accumulated fluences and corresponding SEE results. No hard or soft reset was needed for the data link to restore normal operation; therefore the SEE events observed were transient effects. At fluence lower than 1×10^{11} protons/cm^2 no SEE events were observed. As fluence increased, a small number of transmission errors were recorded.

TABLE III
PROTON BEAM RUNS AND SEE RESULTS

Run	1	2	3	4
flux (protons/cm^2 /s)	< 6 x 10^{8}	1 x 10^{9}	2 x 10^{10}	5 x 10^{11}
fluence (protons/cm^2)	1 x 10^{11}	3.7 x 10^{12}	7.6 x 10^{13}	1.9 x 10^{15}
SEE-LoL events	0	1	19	200
SEE-bit err events	0	0	4	20
LoL cross-section (cm^2)	< 2.7 x 10^{-11}	2.7 x 10^{-13}	2.5 x 10^{-13}	1.1 x 10^{-13}
bit err cross-section (cm^2)	<2.7 x 10^{-11}	< 2.7 x 10^{-13}	5.3 x 10^{-14}	1.1 x 10^{-14}

The absolute majority of events are frame errors, caused by loss of synchronization of the link (LoL). Only few events were shown as data corruption (Bit error). This indicates that the analog circuitry in GOL chip is more susceptible to proton irradiation than the digital circuitry [6]. All loss-of-synchronization errors, characterized by detected frame control bits changing from valid data to error propagation, endured for a number of consecutive frames. For the purpose of analysis, each block of consecutive frame errors was treated as one event. SEE cross-section is derived from the number of SEE events registered during a period of time divided by fluence. Cross-section derived from the highest flux run is smaller than cross-sections derived from the lower flux runs, but is within 3σ variance determined by the number of error samples. We evaluate the proton irradiation transient SEE cross-section to be $(2.5\pm0.6)\times10^{-13}$ cm^2 for loss of synchronization events and to be $(5.3\pm2.6)\times10^{-14}$ cm^2 for bit corruption events.

IV. SUMMARY

A test system to characterize the radiation hardness of a Gigabit per second serializer (GOL) has been developed. Two GOL chips were exposed to total ionizing dose of 100 Mrad(Si) with no functional degradation. Single event effect cross-sections are calculated to be $(2.5\pm0.6)\times10^{-13}$ cm^2 for loss of synchronization events and $(5.3\pm2.6)\times10^{-14}$ cm^2 for bit corruption events.

V. ACKNOWLEDGMENT

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