

A Serializer ASIC for High Speed Data Transmission in Cryogenic and HiRel Environment

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Abstract—A high speed 16:1 serializer ASIC has been developed using a commercial 0.25 μm silicon-on-sapphire CMOS technology. At room temperature the ASIC operates from 4.0 to 5.7 Gbps with power consumption of 463 mW. The total jitter is 62 ps at the bit error rate of 10^{-12} at 5 Gbps. A 200-MeV proton beam test indicates that the ASIC is suitable for high energy physics applications. A liquid nitrogen temperature test indicates that the ASIC may be used at cryogenic temperature applications. The reliability of the serializer at liquid nitrogen temperature is to be studied. A 6-lane serializer array with 10 Gbps/lane with redundancy capability is under development.

I. INTRODUCTION

The optical data links for the ATLAS liquid argon (LAr) calorimeter between the front-end boards (FEBs) and the back-end electronics operate at 1.6 gigabit per second (Gbps) per fiber channel [1]. In the ATLAS LAr calorimeter readout electronics upgrade for the sLHC, it is proposed to remove the analog Level-1 trigger sum from FEB and transmit continuously digitized data off the detector. Consequently, the data rate of the optical links increases from 1.6 Gbps to about 100 Gbps per FEB. The total data rate of 1524 FEBs reaches 150 Tbps [2]. However, the data rate of G-Link or GOL [3] currently used in high energy physics experiments is no more than 1.6 Gbps, too slow for the upgrade. Thus for the LAr calorimeter readout system, a high speed serializer is required. Moreover, the running experiences of ATLAS experiment indicate that optical links in radiation environment are still fragile [4]. When an optical link carries multiple Gbps data stream, it is very important to improve the link reliability with redundancy.

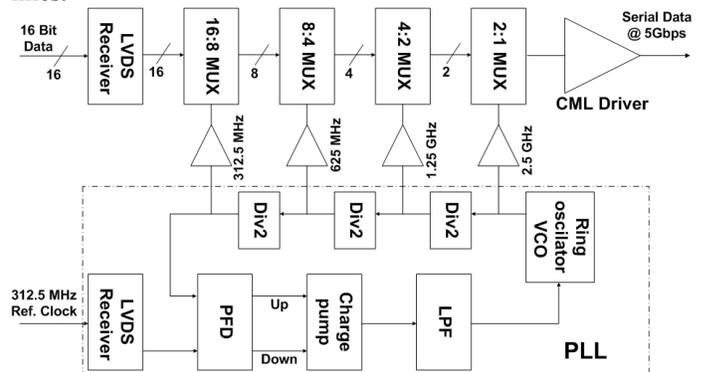
A Liquid Argon Time Projection Chamber (LAR-TPC) has full 3-D event reconstruction capability with sub-millimeter position resolution, larger than 90% electron-photon separation, and particle energy threshold as low as 1-2 MeV, making it an ideal neutrino physics detector [5]. A 20,000-ton LAR-TPC has been proposed to be built as a far-site detector of the long-baseline neutrino experiment (LBNE). The increase of the input capacitance and the input equivalent noise makes it impossible to build a large fiducial volume detector with all preamplifiers located outside the cryostat at room temperature. Moreover, large amount of cables and feedthroughs increases cost, thermal load, and the possibility of outgassing and leaks. Therefore, a cold front-end electronics scheme has been proposed, in which all preamplifiers, shaping amplifiers, analog to digital converters, zero suppression, buffers, and

data multiplexing are put in liquid argon. All devices inside the cryostat have to operate at liquid argon temperature (89 K) for over 15 years without any access for repair or replacement.

Based on the commercial 0.25 μm silicon-on-sapphire (SOS) CMOS technology we have developed a 5 Gbps 16:1 serializer, named as LOCs1 [6]. LOCs1 is the first step towards optical links for the readout upgrade of the ATLAS LAr calorimeter for the super LHC. LOCs1 is also a candidate for the optical data links proposed to read out the experimental data in the LArTPC of LBNE. In this paper we present the design and the test results of LOCs1 at room temperature, in 200-MeV proton beam, and at liquid nitrogen temperature.

II. DESIGN OF THE SERIALIZER

The serializer consists of a serializing unit, a phase lock loop (PLL) clock generator and a current-mode-logic (CML) driver as shown in Fig. 1. The serializing unit multiplexes 16 bit parallel low-voltage differential signaling (LVDS) data into a serial bit stream. The serializer unit extends 2:1 multiplexers to a 16:1 one with binary tree architecture. Only the last 2:1 multiplexer needs to be optimized to work at the highest speed or 2.5 GHz. Two complimentary 2.5 GHz clock signals are required to speed up the D-flip-flop in the last 2:1 multiplexer. To achieve good immunity from the single-event effects (SEEs), we use large size transistors and static D-flip-flops in the whole design. With a 312.5 MHz reference clock input, the PLL clock generator provides 2.5 GHz, 1.25 GHz, 625 MHz, and 312.5 MHz clock signals to the serializing unit. A multiple-loop differential ring oscillator is used to boost the operating frequency of voltage control oscillator (VCO). The PLL loop bandwidth is programmable for adapting different reference clock qualities. The PLL can be configured to lock to either the rising or falling edge of the reference clock. This edge-selection feature is useful for the users to latch data with optimal timing. The CML driver can drive 50 Ω transmission lines.



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Fig. 1. Block diagram of the serializer.

The micrograph of the serializer ASIC is shown in Fig. 2. The serializer occupies about 50% area of a $3 \times 3 \text{ mm}^2$ die. All the I/O pins have electrostatic discharge (ESD) protection except the high speed serial data output pins. The die also includes an LC-tank-based PLL (LCPLL) operating at near 5 GHz. The LCPLL will be used in the next generation of the 10-Gbps serializer array which is discussed in Section IV.

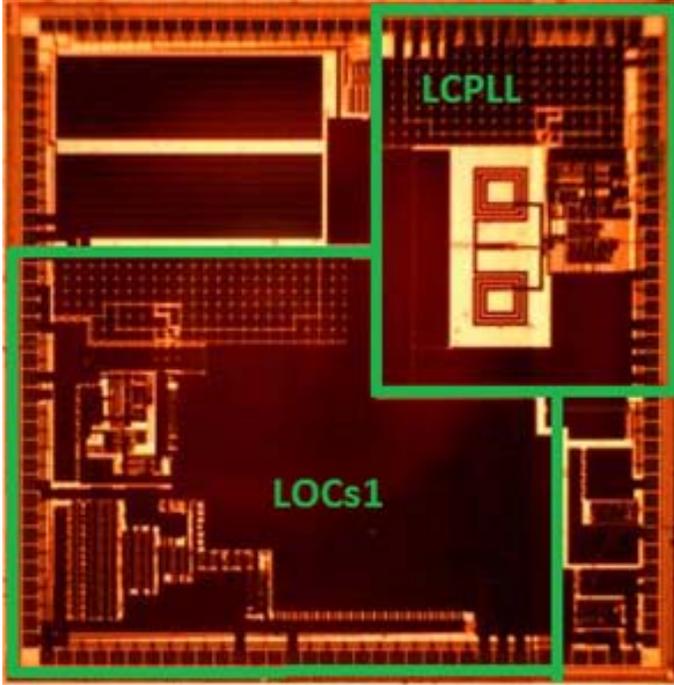


Fig. 2. Die micrograph.

III. TEST RESULTS

A. Laboratory Test

The test setup is shown in Fig. 3. In the laboratory test, a field-programmable gate array (FPGA) based board provides 16 bit parallel data and a clock signal to a dedicated chip carrier board through a twisted pair cable. We measured the high speed serial data parameters through the SMA connectors on board with a high speed real time oscilloscope or a bit error rate tester (BERT). An eye diagram is shown in Fig. 4. The eye mask is adapted from the 4.25 Gbps Fibre Channel standard and scaled to 5 Gbps. We performed jitter measurements with 2^7-1 pseudorandom binary sequence (PRBS) data pattern using oscilloscope software (Tektronix TDSJIT3). Using a commercial BERT (Anritsu Model MP1764C), we measured the bathtub curves. A bathtub curve is shown in Fig. 5.

Among the 12 assembled carrier boards, seven boards work and the other 5 boards do not. Four carrier boards have power supply problems and one board has one stuck bit in the input data. We are going to investigate in the future whether these problems are from ASIC fabrication or wire bonding.

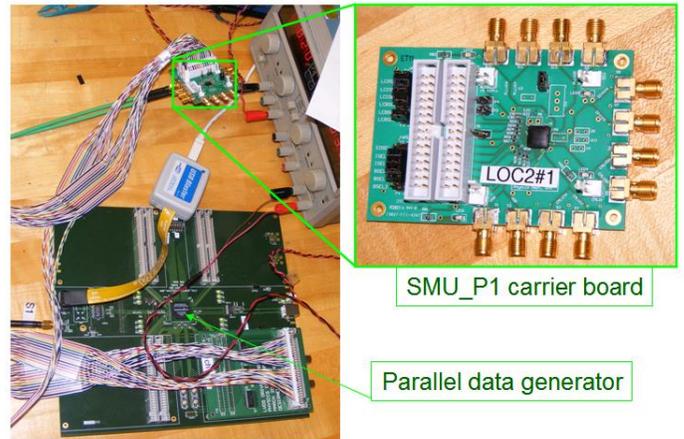


Fig. 3. A picture of the test setup

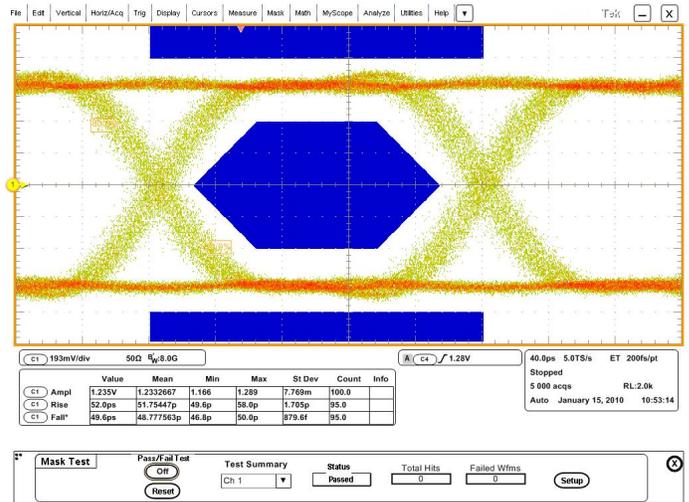


Fig. 4. Eye diagram at 5 Gbps.

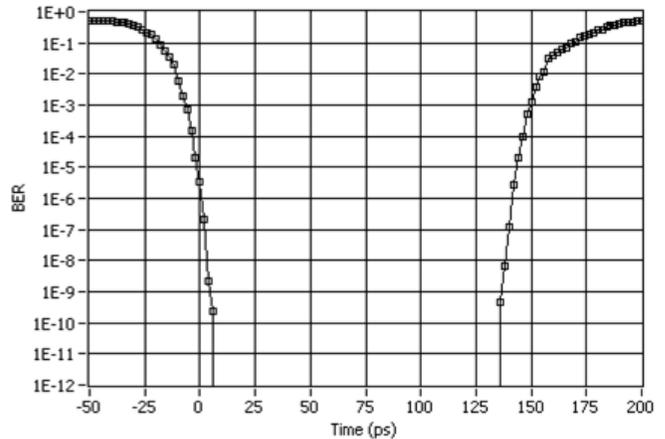


Fig. 5. Bathtub curve at 5 Gbps.

The bit error rates (BER) of all the seven boards are better than 10^{-12} in the data range from 4.0 to 5.7 Gbps. The average values of the major measured parameters of the seven working boards are listed in Table I. All parameters are measured at 5 Gbps except the upper and lower working limits.

TABLE I. AVERAGE VALUES OF THE MEASURED PARAMETERS OF SEVEN WORKING BOARDS

Parameters	Measured results
Output Amplitude (peak-peak, V)	1.16
Rise time (20%–80%, ps)	52.0
Fall time (20%–80%, ps)	51.9
Total jitter at BER of 10^{-12}	61.6
Random jitter (RMS, ps)	2.6
Deterministic jitter (peak-peak, ps)	33.4
Eye opening at BER of 10^{-12} (ps)	122
Power consumption (mW)	463
Upper working limit (Gbps)	3.9
Lower working limit (Gbps)	5.9

We also measured the jitter tolerance with a VBERT, a custom BERT [7]. During the measurements, LOCs1 is the serializer and an Altera Stratix II GX based board works as the deserializer and the error detector. The test result is shown in Fig. 6. With sinusoidal jitter injected at the reference clock of LOCs1, the measured jitter tolerance at BER of 10^{-12} and 5 Gbps is larger than 1.8 unit intervals (UI) when the injected jitter frequency is from 0.7 to 1.56 MHz. The measured jitter tolerance is larger than that specified in the Fibre Channel standard [8], suggesting that the link is robust and not sensitive to the reference clock jitter.

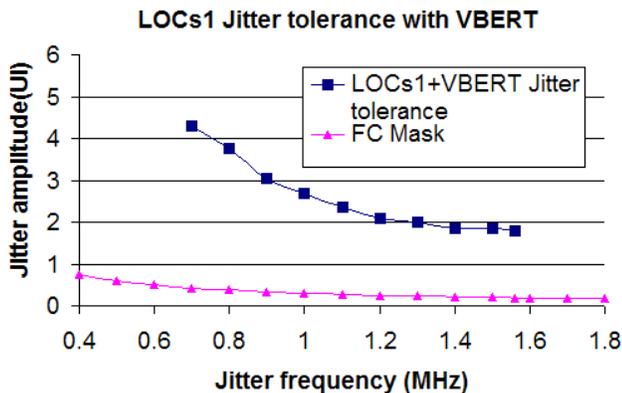


Fig. 6. Jitter tolerance.

B. Radiation Test

We performed a radiation test with a 200 MeV proton beam at Indian University Cyclotron Facility. The test setup is shown in Fig. 7. The VBERT system for online error detection was placed in an area shielded by lead bricks. We put two LOCs1 carrier boards in the beam and another one in the shielded area as a reference. To test the possible angle effects, the angle between the beam incident direction and die surface normal was set at 0, 30, 45, or 60 degree during the radiation test. The boards accumulated 90% fluence when their angles were kept at 60 degree. Because the number of the single-event upsets (SEUs) were small, we did not observe any statistically significant dependence on angles.



Fig. 7. A picture of the setup of radiation test.

The test had lasted for 12 hours in the beam and we kept the test system running for 15 hours after the beam off. We did not observe any bit error in the annealing time. We monitored the power supply current of the serializers during the test. The current change is shown in Fig. 8. The currents changed less than 6% during the beam time and annealing time. This means the total ionizing dose (TID) effects are negligible for our application. We observed two types of SEUs: single bit errors and synchronization errors. The numbers of the observed SEUs are shown in Table II. We observed five single bit error events in total which did not affect the link status afterwards. The extrapolated BER for the single bit errors is 1.6×10^{-18} at sLHC ATLAS LAr calorimeter. When a synchronization error event occurred, there were a burst of bit errors in a short duration. After the burst of bit errors, the received data had one bit shift comparing to the generated PRBS data for error checking in the error detector. The bit shift was removed when the receiver was reset for a word alignment. The duration distribution of the burst errors is shown in Fig. 9. Because the burst of bit errors lasts only several tens bits, for each synchronization error event, the link can be recovered on the receiver side without many bit loss. The extrapolated number of synchronization error events is less than 3 at the ATLAS LAr calorimeter in the whole sLHC life time.

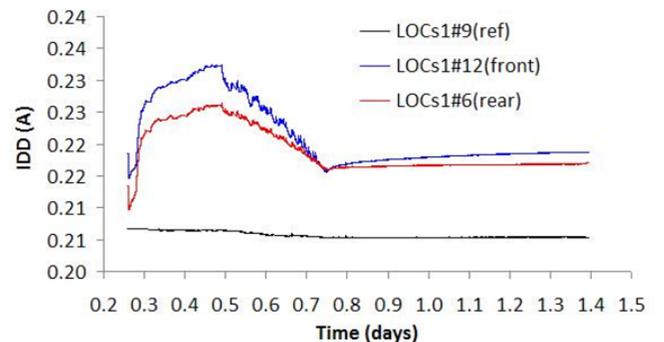


Fig. 8. The power supply current change during the test and during annealing time

TABLE II. OBSERVED NUMBER OF SINGLE-EVENT ERRORS

BOARD#	# OF SINGLE BIT ERRORS	# OF SYNC. ERRORS
6	0	16
12	5	8

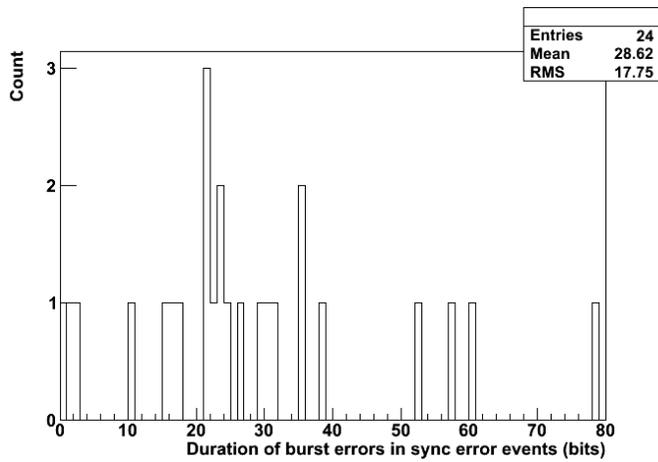


Fig. 9. The duration distribution of burst errors in synchronization error events

C. Cryogenic Test

We have tested the serializer at liquid nitrogen temperature. The test setup is shown in Fig. 10. The serializer is attached at one end of a stepping motor system which is controlled by a computer. A Dewar which contains liquid nitrogen is put on the floor just below the end of the stepping motor system. The temperature depends on the distances between the serializer and the liquid nitrogen surface. The temperature of the serializer is monitored using a temperature sensor attached near the serializer.



Fig. 10. A picture of the setup of cryogenic test.

The eye diagrams of the serializer at room temperature and liquid nitrogen temperature (77 K) are shown in Figs. 11(a-b). The serializer at 77 K has wider eye opening, faster transient time, smaller jitter and larger amplitude than at room temperature.

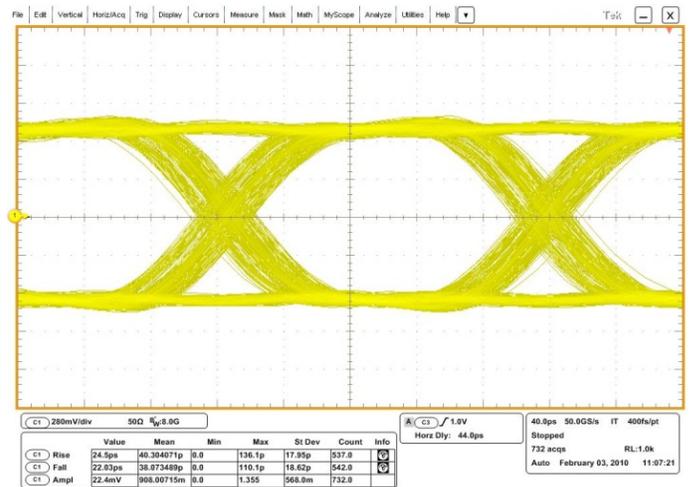


Fig. 11(a). Eye diagram at 5.2 Gbps and room temperature.

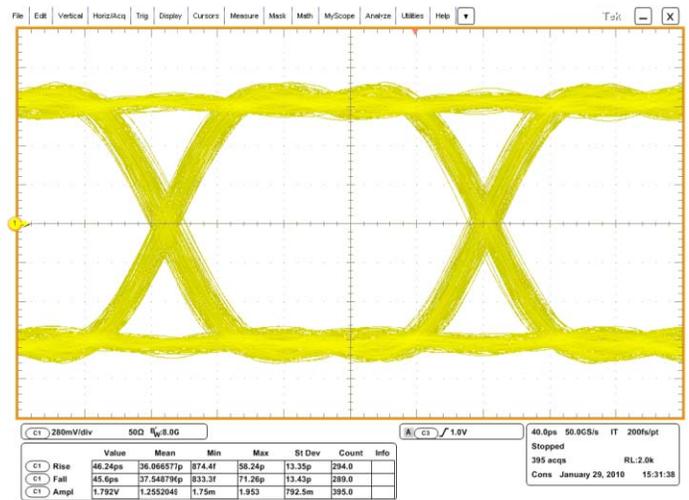


Fig. 11(b). Eye diagram at 5.2 Gbps and liquid nitrogen temperature.

Due to hot carrier effects, chip reliability may be reduced at cryogenic temperature [9-10]. Low power supply voltage may mitigate the hot carrier effects and hence increase its reliability. The eye diagram of the serializer operating at 1.8 V is shown in Fig. 12. The nominal power supply voltage is 2.5 V. It is possible to increase the reliability at cryogenic temperature by operating this chip at a lower power supply voltage. The lifetime reliability of the serializer at liquid argon temperature will be studied in the future.

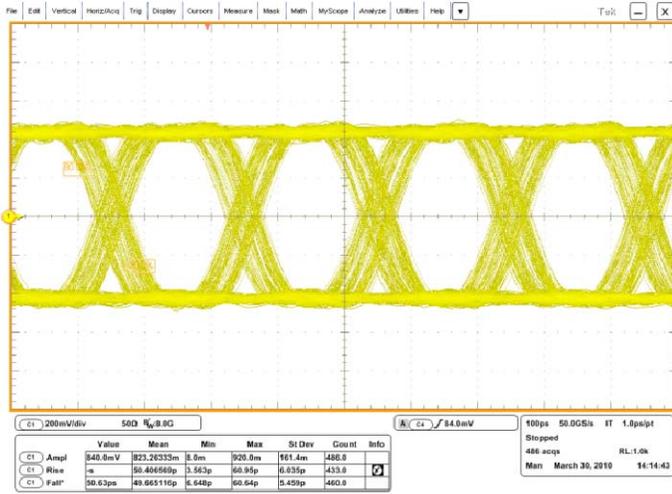


Fig. 12. Eye diagram at 5.0 Gbps and 1.8 V power supply voltage.

IV. FUTURE WORK

To meet the challenge of 100 Gbps data rate per FEB, parallel optical links are studied. The parallel optical links use two 6-lane 10 Gbps serializer array chips and a 12-way fiber ribbon for each FEB. By adding a switch network on the input data path of the serializer array, one of the 6 serializers can be configured as a redundant channel to improve the optical link system reliability, as shown in Fig. 13. The serializer marked in grey color is configured as a redundant channel.

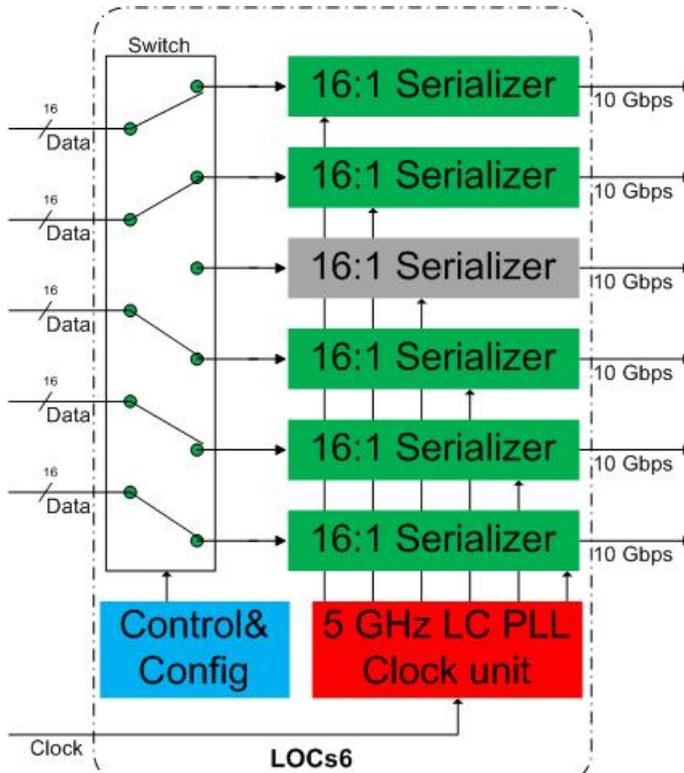


Fig. 13. Block diagram of a 6-lane serializer array.

The critical component of the serializer array is a 10 Gbps serializer. By using the same architecture shown in Fig. 1, the 5 GHz PLL clock unit, the clock buffer, the high speed divider, the last stage 2:1 multiplexer and the CML driver need to be redesigned. We have implemented an LCPLL on the same die as LOCs1 and the test results indicate that it can provide near 5 GHz low jitter clock signal with low power consumption. The CML driver used in the LOCs1 is measured to be able to work up to 8.5 Gbps with no bit error. We plan to improve the bandwidth of the CML driver using the inductive peaking technology. The design of the CML buffer has started and the preliminary simulation results show that the approach is promising.

V. CONCLUSION

A 5 Gbps 16:1 serializer ASIC in a commercial 0.25 μm SOS CMOS technology has been developed. Laboratory test indicates that we have achieved the design goals. Irradiation test indicates that the ASIC meets the application requirements. Cryogenic test indicates that the ASIC may be used in cryogenic temperature. A 6-lane serializer array with 10 Gbps/lane with redundancy capability is under development.

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