Single Event Effects in a 0.25 μm Silicon-On-Sapphire CMOS Technology

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35-word Abstract:

A test chip has been designed using standard and radiation tolerant techniques in a 0.25μm Silicon-On-Sapphire process. The test chip has been irradiated under a 230 MeV proton beam. The SEE results are reported.

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I Introduction

Single Event Effects, otherwise known as SEE's, are undesired effects caused by single energetic particles passing through a given medium. These effects are generally categorized into three distinct occurrences: single event upset (SEU), single event latch-up (SEL), and single event burnout (SEB). SEU's are non-detrimental transient soft errors which happen during device operation. In particular, SET or single event transient typically happens in combinatorial logic where an energetic particle passing through the circuit causes a logic state to change. This error is then propagated throughout the circuit and seen on the output. It is also possible for multiple bits to change logic states, resulting in errors at the output. SEL's on the other hand results from an energetic particle passing through a device, turning on parasitic bipolar elements. However, it is not possible for a bipolar element to form between the CMOS wells and substrate in Silicon-On-Sapphire(SOS) technologies. Thus, no latch up can occur in Silicon-on-Sapphire processes and it is not an issue in this study. Finally, SEB's are hard catastrophic effects caused by highly induced current states over time, leading to permanent device failure. In this study, we examined the effects of SEE's on Peregrine's 0.25μm Silicon-On-Sapphire (UltraCMOS®) technology.

II Experimental Setup

A test chip has been designed using standard and radiation tolerant techniques in Peregrine's Semiconductor 0.25μm Silicon-On-Sapphire (UltraCMOS®) process. The test chip was also used in a TID/total dose study reported in [1]. Peregrine's 0.25μm (UltraCMOS®) technology used in the test chip have the following features:

VDD	2.5V
Gate Oxide Thickness	6 nm
Process	0.25μm Silicon-on-Sapphire(UltraCMOS®)
Device isolation	LOCOS
Interconnectivity	3 metal layers
NMOS polysilicon gates doping	P+
PMOS polysilicon gates doping	N+

Table 1. The Technology features of the test chip

The test chip contains ring oscillators, PLL components (PFD, VCO, divider), a matrix of various sized NMOS and PMOS transistors, logic gates, current mirrors, passive components and shift registers, as seen in Figure 1.

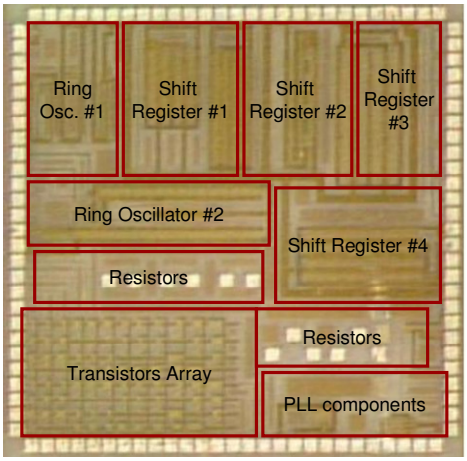

Figure 1. Image of the fabricated Test Chip (Dimensions: 3mm x 3mm)

To test the effect of SEU's and SEB phenomena, we designed a series of shift registers and latches that are operational during online radiation tests.

Shift Registers

On the test chip, we designed variety of shift registers, each comprised of multiple stages of D-Flip Flops connected in a chain format. Figure 2 is the schematic of the latch used in the D flip flops:

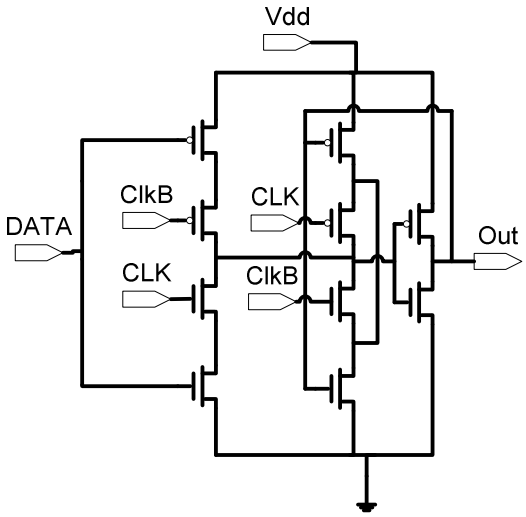

Figure 2. Latch used in DFF

The types of shift registers are made up of the following:

(1) Standard geometry transistors.
(2) Enclosed layout transistors.
(3) Resistively hardened cells.

The standard geometry and enclosed geometry shift registers are made up of 32 stages of D-Flip Flops connected in chain format. The sizes of both the PMOS and NMOS transistors in these registers are kept consistent for comparison purposes. The enclosed geometry transistors were manually drawn based on a numeric model given in [2].

The resistively hardened shift registers had a total of 32 stages divided into 8 sub sections. Each subsection has a resistance that doubles its previous stage. The resistor sizes are: 1,2,4,8,16,32,64, and 128 kOhm. The resistors were placed in the output and feedback path of the DFF. Figure 3 depicts the resistively hardened DFF schematic:

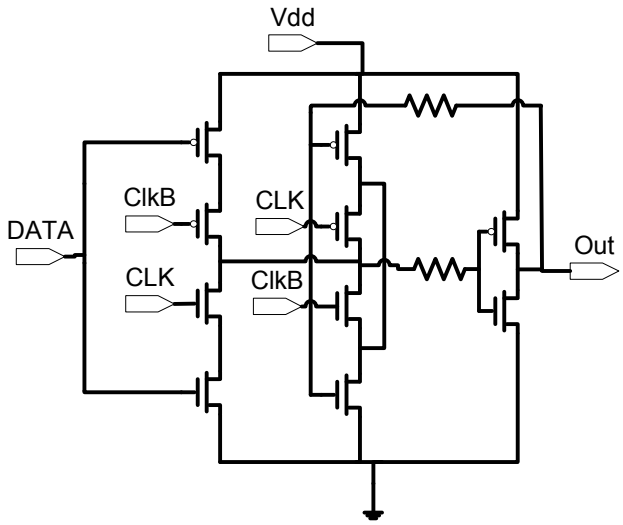

Figure 3. Resistively Hardened DFF. Resistors in Output and Feedback Path [3]

The scheme here is to slow the response in between each node so that the circuit itself does not have time to respond to the radiation induced single event effects [3].

The purpose of the standard geometry based shift register is to provide a basis for comparison. The enclosed geometry based shift register depicts an alternative design technique via layout. The use of enclosed layout in this experiment was to explore TID effects due to leakage current. Resistive hardening presents an alternative circuit level scheme to mitigate SEE effects.

Latch with Set Free Inverter Chain

We designed a chain of latches based on SET free logic as seen in Figure 4:

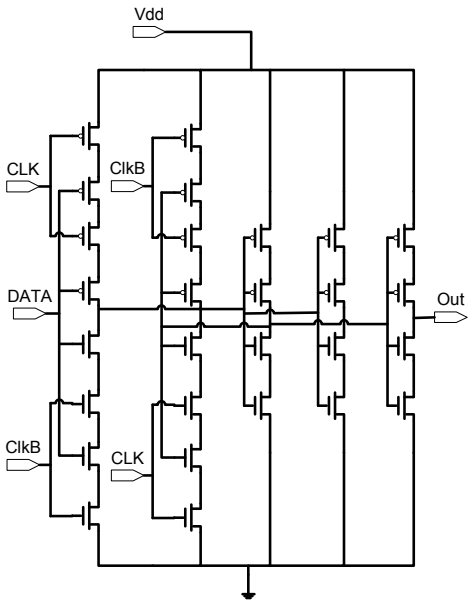

Figure 4. Latch with SET free inverter[4].

The idea for SET free logic is to construct logic elements that will not allow single event transients to generate and thus propagate to the outputs. This method is similar to TAG and guard ring topologies [4]. Thus, the SET effect is eliminated.

To accomplish the online test, a PRBS or pseudo random bit stream, is written into the data input of each test element via a FPGA at 40 Mb/s. The bits are then read back from the shift registers and compared with a similarly seeded PRBS. Any differences between the inputs and outputs are reported as errors. Figure 5 depicts the test scheme.

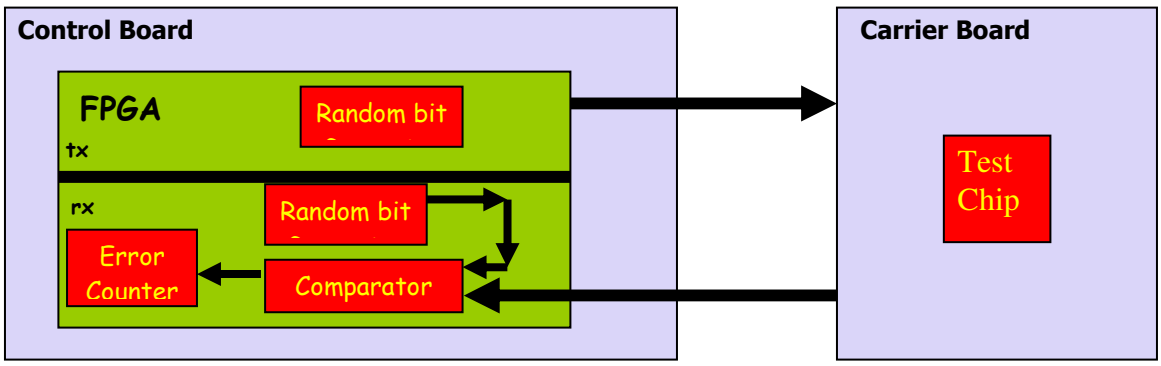

Figure 5. Online Test Scheme

For the resistively hardened shift register, PRBS data is written in at a rate of 40 Mb/s. The data is then stored inside the circuit for a period of 1 second. Afterwards, it is read back into FPGA to check for errors. In addition, we monitor current consumption of all test elements with a multi-channel digital multimeter.

IV Measurement Results And Discussion

An online test was done on the shifter registers and latch chain at dose of 100krad (Si) under a 230 MeV proton beam for up to 3 hours. The top left illustration of Figure 6 depicts the current consumption of the test elements. The top right of Figure 6 shows the fluence over time. The bottom illustrations of Figure 6 depict the errors reported by the FPGA. Relating to the functionality of our test structures, there was no significant current change that inhibited device operation. Likewise, the FPGA reported no errors as seen in Figure 6.

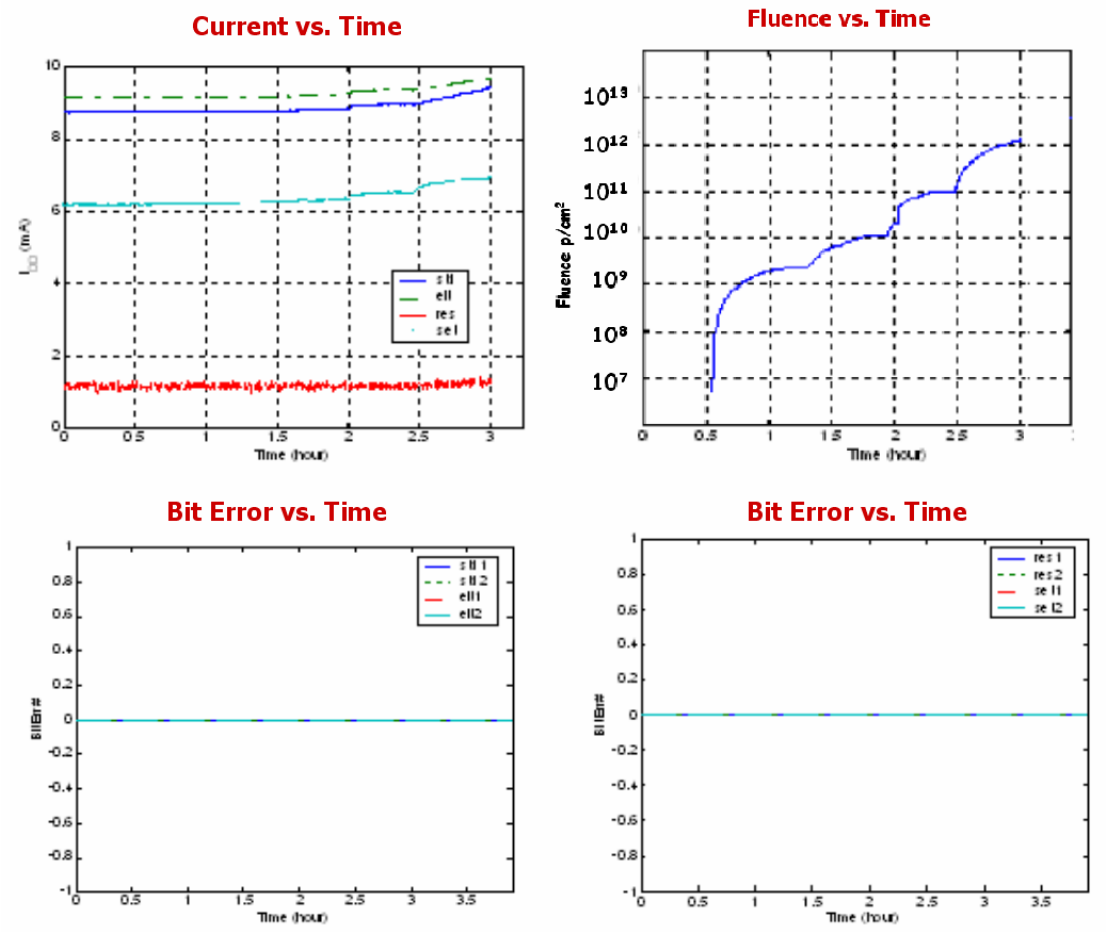

Figure 6. Test Results Shown. Current Consumption (Top Left), Fluence(Top Right) Standard Geometry and Enclosed Geometry Based Shift Register Errors(Bottom Left), Resistive Hardening and SET free logic shift register errors (Bottom Right)

When comparing standard geometry based shift registers to enclosed geometry based shift registers, there was no difference in functionality and SEE immunity. In addition, since the standard geometry based shift register worked error free for the given radiation period, the resistive hardening technique showed no further benefit in relation to SEE immunity.

From the results of the test elements up to 100krad(Si), we report that typical SEU's and SEB's were not seen in our experiment on Peregrine's 0.25 μm (UltraCMOS®) technology. Table 2 shows fluence, error count # and cross section data for the different type of test elements in our experiment.

Test Element Type	Fluence (proton/cm^2)	Error Count #	Cross section (cm^2)
Std Shift Register	1.8×10^{12}	0	$<5.6\times10^{-13}$
ELT Shift Register	1.8×10^{12}	0	$<5.6\times10^{-13}$
Res. Hard Shift Register	1.8×10^{12}	0	$<5.6\times10^{-13}$
SET free logic latch	1.8×10^{12}	0	$<5.6\times10^{-13}$

Table 2. Fluence, Error Count # and Cross Section Data for Test Elements

Based on the results of our experiment, we have shown that Peregrine's 0.25 μm Silicon-On-Sapphire (UltraCMOS®) process has exhibited SEE immunity in certain test structures up to 100krad(Si) of radiation. The data we have collected shows that the special radiation tolerant design techniques employed do not perform any different from standard design techniques in relation to SEE immunity up to 100krad(Si) of radiation.

When the dose rate was increased to limits well beyond operating specifications and reasonable limits of circuit survivability, the resultant effects were major increases in current consumption and errors occurring on test elements.

V Conclusion

While radiation tolerant design techniques have been proven to help mitigate SEE effects, we have shown that these techniques might not be necessary if the correct technology is used. It is important to note that the use of these special design techniques depend on a case by case basis. There could be instances where these techniques prove useful. However from this study, standard design techniques in 0.25μm Silicon-on-Sapphire (UltraCMOS®) technology shows to produce similar functionality to that of radiation tolerant design techniques in relation to SEE immunity.

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