The AD9042 Evaluation System

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Abstract: The 12-bit analog-to-digital converter AD9042 is used in the front-end readout system of the ATLAS Calorimeter. Randomly selected chips from each of the production lots must be qualified for their radiation hardness. An evaluation system was developed to measure the dynamic performance of the qualification samples in each lot. Measurement results of 10 sample chips demonstrated the ultra low noise performance of the evaluation system.

1 Introduction

The AD9042 is a high-speed monolithic 12-bit analog-to-digital converter (ADC) produced by Analog Devices, Inc. (ADI) [1]. It is used in the ATLAS experiment in the radiation environment as a component of the on-detector front-end readout system for the calorimeter [2]. It should maintain its performance throughout the lifetime of ATLAS. The AD9042 is fabricated in a high-speed complementary bipolar process and, in principle, should possess sufficient intrinsic radiation hardness to satisfy the requirements posed by the experiment. The radiation requirements are based on the total dose accumulated during the normal operations of the experiment throughout its expected lifetime of 10 years [3]. For the bi-polar technology, small variation of the production process may introduce sensitivity for the radiation damage. The AD9042 is not sold with any guarantee of a radiation hardness, and therefore, its radiation hardness must be evaluated for each production batch.

Previous radiation hardness study of the AD9042 demonstrated that its post-radiation performance was uniform and did not change from wafer to wafer within a production lot [4]. Consequently, random samples may be used to qualify a lot. The following acceptance procedure has been approved by the ATLAS collaboration and by ADI: The ADCs production will be separated into lots of about 7500 chips. About 50 chips will be selected at random from each lot as the qualification samples. The qualification samples will be measured for their dynamic performance, including the signal-to-noise ratio, the worst spur and the reference voltage. Then the samples will

be exposed to the gamma and neutron beams, corresponding to the integrated doses of 1 MRad of ionizing radiation and 2×10^{13} neutrons/cm^2, where the mean neutron energy is approximately 1 MeV. After irradiation, the performance of the samples will be measured again. The lot will be accepted or rejected based on the post-radiation performance.

The authors of Ref. [4] achieved a typical signal-to-noise ratio of 63 dB instead of the nominal 68 dB specified in the data sheet [1]. This indicated that an additional noise was introduced in the evaluation system. Therefore, a special, low noise evaluation system had to be developed.

2 The evaluation system setup

The purpose of the evaluation system is to measure the reference voltage and the dynamic performance, including the signal-to-noise ratio and the worst spur. A digital multimeter can measure the reference voltage. In order to measure the signal-to-noise ratio and the worst spur, a precise sine wave signal is used as the input to the ADC. The ADC samples and digitizes the sine wave. The digital signals are transmitted to a computer, transformed into the frequency domain and analyzed. The performance characteristics of the ADC are calculated based on the harmonics and on the noise as compared to the corresponding component at the input frequency [5].
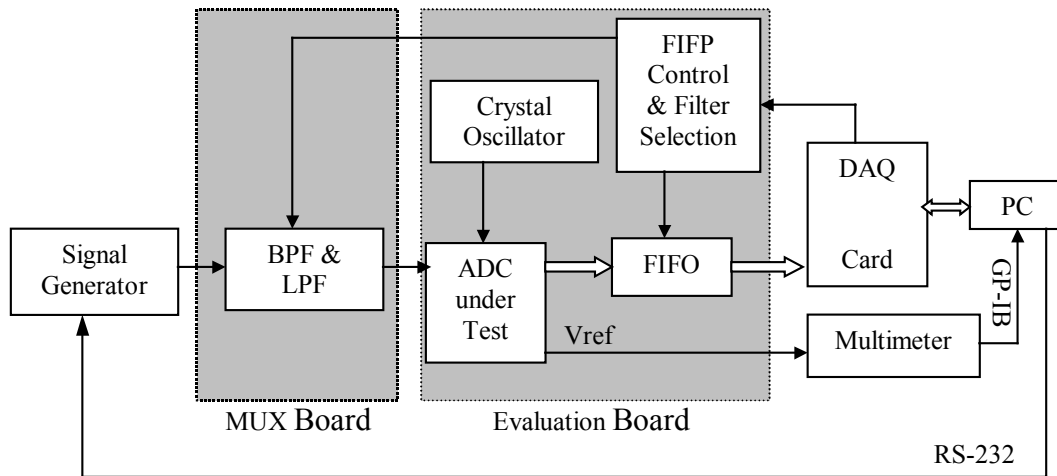

Figure 1 The block diagram of the evaluation system

The block diagram of the evaluation system is shown in Figure 1. The sine wave generator produces the analog input signal. The band-pass filters (BPF) and the low-pass filters (LPF) purify the analog signal (see next section for more detail). The crystal oscillator generates the clock used by the ADC to sample the analog signal. The ADC samples and digitizes the analog signal. Then the digital output is transmitted to a computer via a data acquisition (DAQ) card, the HS-32-DIO from the National Instruments Corporation. Since the data rate is too high for the DAQ card, the data is buffered in a 64k first-in-first-out (FIFO) memory chip, IDT72285 from Integrated Devices Technology, Inc. A complex programmable logic device (CPLD), EPM7128BTC100-7 from the Altera Corporation, is used to control the relative timing among the ADC, the FIFO and the DAQ card. The ADC, the FIFO, the crystal oscillator and the CPLD are located on one newly designed board (the Evaluation Board in Figure 1). The output data is analyzed off-line. We calculate the signal-to-noise ratio and the worst spur. A digital multimeter 33410A from Agilent Technologies, Inc. is used to monitor the reference voltage and to transmit the results to the computer via a GPIB card. The frequency and amplitude of the sine wave is set through a serial port. The software for the measurement procedure is written in LabVIEW.
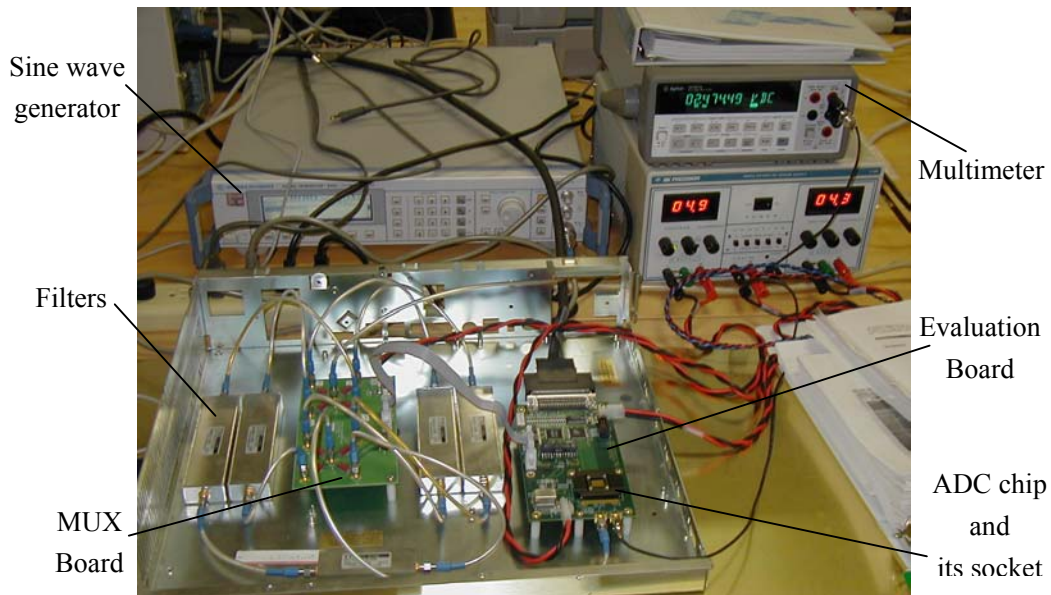

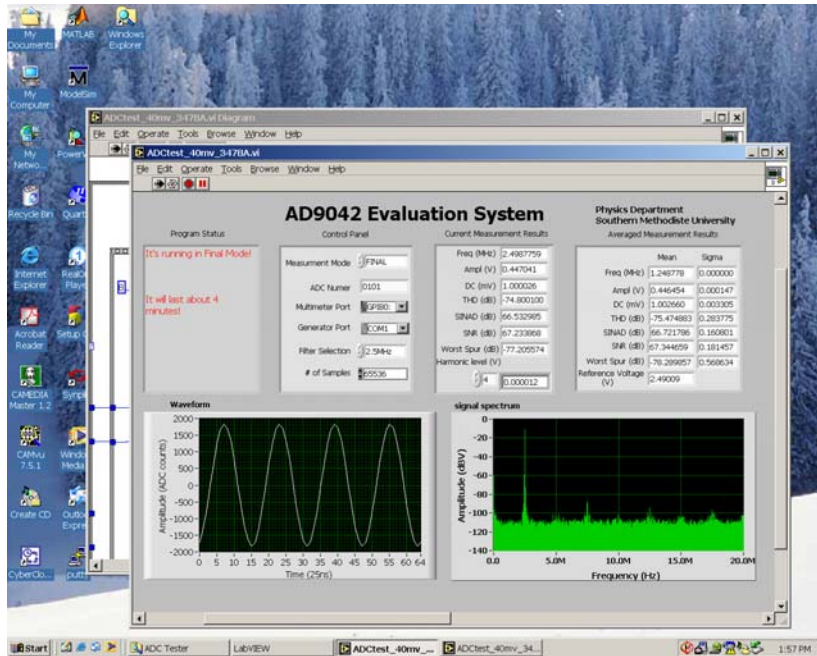Figure 2 A photograph of the evaluation system

Figure 3 The graphical user interface of the software

A photograph of the evaluation system is shown in Figure 2. A typical example of the graphical user interface of the evaluation system is shown in Figure 3.

3 The design of the evaluation system

For the measurement of the signal-to-noise ratio and of the worst spur of the ADC, we made an assumption that all noise and the unwanted harmonics come from the ADC and not from the evaluation system itself. Since the ADC is supposed to have a very low noise and harmonics (typically a SNR of 68 dB and a worst spur of 78 dBc), the evaluation system must have even lower noise and harmonic contribution. In general, the noise and harmonics may come from the impurity of the input signal, from the noise of the Evaluation Board, or from the sampling clock jitter. Therefore, the evaluation system must be carefully designed to have (1) a sine wave with ultra low noise and harmonics, (2) a sampling clock with ultra low jitter, and (3) an Evaluation Board with ultra low noise.

3.1 The signal generator and filters

As far as we know, no commercial signal generator provides a sine wave in a wide

frequency range (1 MHz ~ 10 MHz) with harmonics lower than the AD9042. A band-pass filter is necessary to purify the signal. In some cases (e.g., for 9.6 MHz sine wave in our system), the harmonics are still too big after a band-pass filter. Therefore, we use a low-pass filter with a zero located at the second harmonic frequency of the sine wave that follows a band-pass filter and reduces the harmonics.
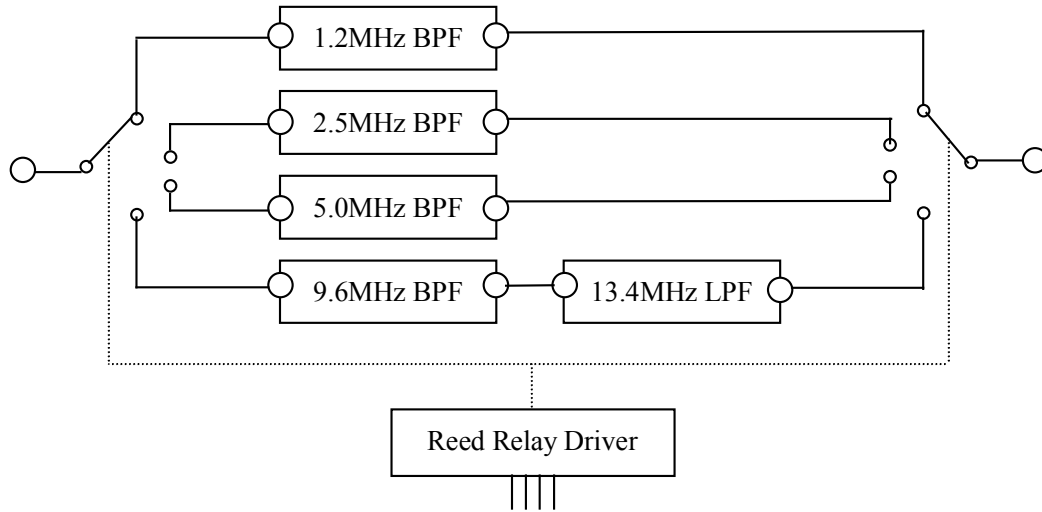

Figure 4 The architecture of the MUX Board

For our setup the signal generator SML-01 from the Rohde-Schwartz Corporation was chosen because of its exceptional low phase noise, flat frequency response and reasonable harmonic performance. Q70 series band-pass filters with minimum 10% bandwidth and J97 series low-pass filters from the TTE Corporation were selected.

Each filter purifies the sine wave of one frequency. The analog signal frequency is below 10 MHz and is sampled at 40 MHz in ATLAS. Therefore, we chose to measure the AD9042 at four frequencies, 9.6 MHz, 5.0 MHz, 2.5 MHz and 1.2 MHz. For convenience, a MUX Board was designed to perform measurements by automatically switching from one filter to another. The architecture of the MUX Board is shown in Figure 4. Reed relays with high reliability, high insulation resistance, and shielded coaxial 50 Ω impedance are used to switch between different groups of filters. We use the 9800 series reed relays from the Coto Corporation.

3.2 The Sampling Clock generation

According to the sampling theory, the jitter of the sampling clock will introduce a

wideband noise [6]. For example, the 9.6 MHz sine wave sampled by a clock with 4 ps root-mean-square jitter will introduce an equivalent noise of one least significant bit for a 12-bit ADC. In order to achieve ultra low noise performance, the sampling clock must have an ultra low jitter. The block diagram of the clock generation circuit, a key part of the Evaluation Board, is shown in Figure 5. The XO-400 series crystal oscillator from Vectron International has been selected for our system. It has 0.5 ps root-mean-square jitter. A 1:2 buffer, MC10EP11 from the On Semiconductor Corporation, with a typical 0.2 ps jitter is used to fan-out the clock from the crystal oscillator to the ADC and to the FIFO. All key clocks use positive emitter coupling logical (PECL) differential signals to minimize jitter.
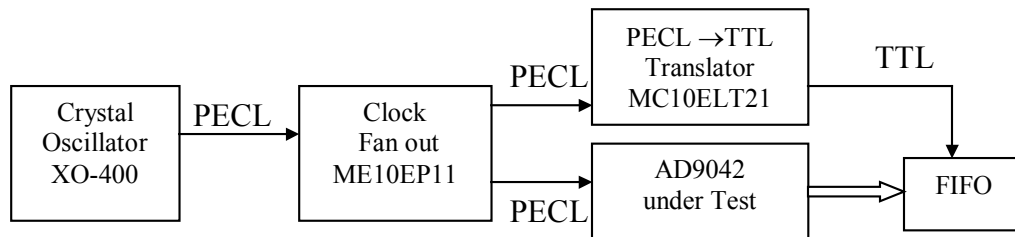

Figure 5 The clock generation circuit

3.3 The Evaluation Board design

The Evaluation Board has 4 layers. The top (first) and bottom (fourth) layers are the routing layers and all key traces are in the top layer. The second layer is the ground plane. The third layer is the power plane that is split into two sections: the digital area and the analog area. The analog signals and the sampling clock of the ADC are referenced to the analog area of the power plane. An Oztek direct contact socket from Kulicke & Soffa, together with the hard-gold-plated PCB, is used to hold the ADC. Cables with SMA connectors are used to connect the sine wave signal generator and the Evaluation Board. All traces that carry the analog and the sampling clock signals are microstrips of 50 Ω impedance. The analog and the digital power supplies are provided separately from a linear power supply. In order to minimize the digital noise from the CPLD, no logic gate changes state while the ADC is sampling and writing data into the FIFO.

4 The application of the evaluation system

Ten sample chips were measured using our evaluation system. The results are shown in Figure 7 and compared with the results measured with ADI's own evaluation system. All measurements were made with an input signal at a frequency of 1.2 MHz or 9.6 MHz and at an amplitude of 1 dB smaller than the full scale.

The SNR and the worst spur results at 1.2 MHz are illustrated in Figures 7 (a) and (b). All results are around the typical values (67.5 dB for SNR and 78 dBc for the worst spur) specified in the data sheet. The SNR results measured using our evaluation system are consistent with the results obtained with ADI's.

Plots shown in Figures 7 (c) and (d) illustrate the SNR and the worst spur results at 9.6 MHz. All results are in agreement with the typical values of 67.5 dB for the SNR and 78 dBc for the worst spur specified in the data sheet. The results measured using our evaluation system appears to have less system noise and harmonic contribution than the results obtained by ADI. The difference between the results obtained here and at ADI is small and may be explained as due to the quality of the input signal. At 9.6 MHz a band-pass filter followed by a low-pass filter is used in our system while only a band-pass filter is used in ADI's system, so the noise and harmonics in our system are expected to be lower than in ADI's system. In both cases, we attribute all noise and harmonics to the ADC chip. The SNR depends on the total noise: the noise from the evaluation system and the noise from the ADC. The case is the same for the worst spur.

(a) SNR @ 1.2MHz and -1dBFS
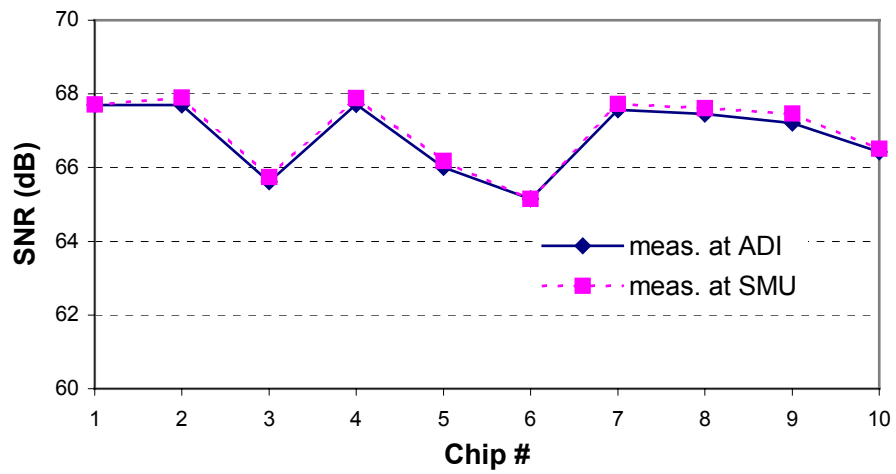
(b) Worst Spur @ 1.2MHz and -1dBFS

(c) SNR @ 9.6MHz and -1dBFS
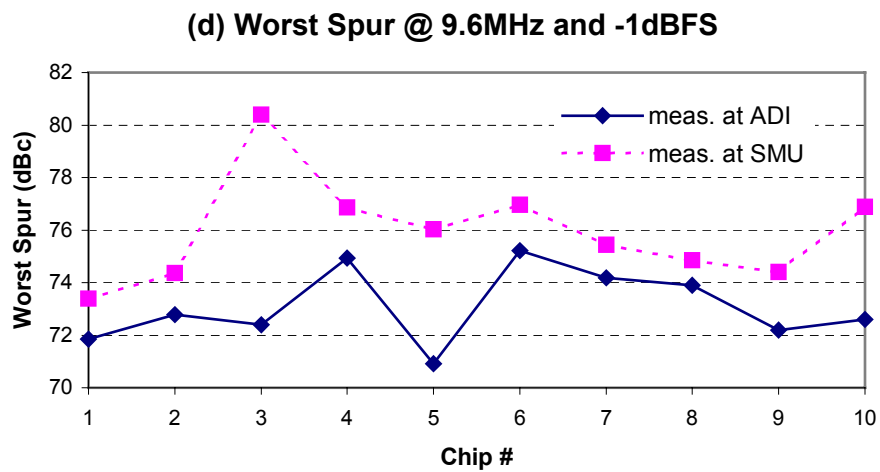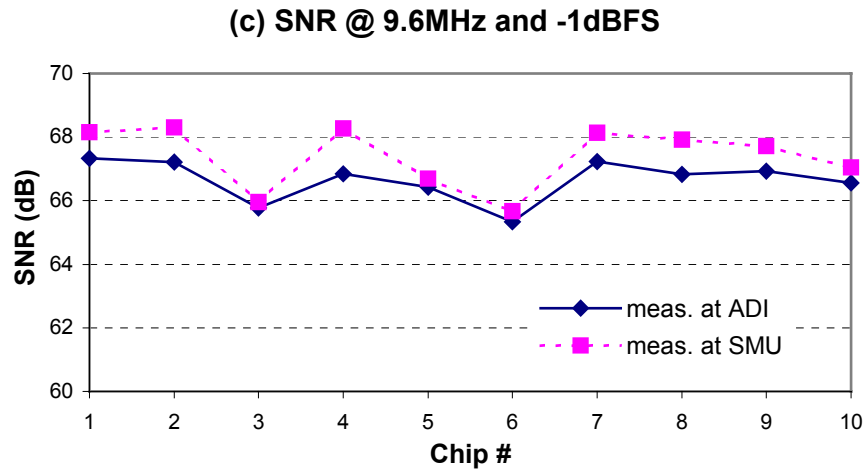

(d) Worst Spur @ 9.6MHz and -1dBFS
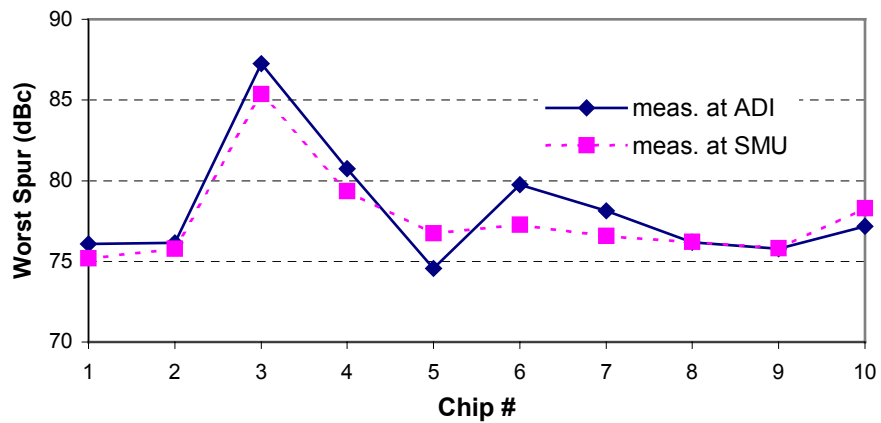
Fig. 7 The comparison of measurements with ADI's results for 10 sample chips

5 Conclusion

An evaluation system was developed to measure the dynamic performance of the AD9042 chip. The measurement results of 10 ADC samples demonstrate that the noise and harmonics associated with the evaluation system is small and does not affect the measurement of the ADC performance characteristics. The evaluation system is now used to qualify the radiation hardness characteristics of the AD9042 chips for the ATLAS experiment.

Acknowledgements

References

[1] Analog Devices, Inc., *AD9042 12-bit, 41 MSPS monolithic A/D converter*, 1996.
http://www.analog.com/Analog_Root/productPage/productHome/0%2C2121%2CAD9042%2C00
.htm.

[2] ATLAS Collaboration, Liquid Argon Calorimeter Technical Design Report,
CERN/LHCC/98-16, 1998.

[3] *ATLAS Radiation Hard Electronics Web Page*
http://atlas.web.cern.ch/Atlas/GROUPS/FRONTEND/radhard.htm.

[4] P. Denes, B. Lev, and R. Wixted, *Radiation hardness evaluation of the Analog Devices AD9042 ADC for use in the CMS Electromagnetic Calorimeter*, Nuclear Instruments and Methods in Physics Research A417, 1998, pp. 371-376.

[5] IEEE Standard 1241-2000, *IEEE standard for terminology and test methods for analog-to-digital converters*, 7 December 2000.

[6] Brad Brannon, *Aperture uncertainty and ADC system performance*, Analog Devices, Inc.
Application Note 501 (Reversion 0).
http://www.analog.com/UploadedFiles/Application_Notes/395652273066884897736516373AN
501.pdf.