A Discussion about the Effects of Substrate Biasing on Radiation Induced Leakage Current During Irradiation in a Silicon-on-Insulator CMOS Technology

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35-word Abstract:

Mechanism that may affect leakage current of SOI MOSFETs by applying an electrical potential to the substrate during irradiation is discussed and presented as a way to mitigate TID effect in high dose rate environment.

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Silicon-on-Insulator (SOI and SOS included) CMOS technology has been a choice for radiation tolerant electronics. This technology has clear advantages over bulk CMOS in removing the mechanism for latch-up and in having smaller single events upset (SEU) cross section [1, 2]. However, the total ionization dose (TID) effect is usually of a concern. This is because that SOI device has back channel leakage [3, 4] that is usually only controlled through special fabrication process. In addition to the back channel, there is edge leakage that is common to bulk CMOS and is usually mitigated through special layout techniques. With the decreasing feature size and the substrate thickness, TID effect may be of less a concern, especially in applications where the dose rate is moderate and when the radiation induced leakage current during high dose rate test can anneal away in room temperature in a proper period of time calculated according to the realistic dose rate in the actual application. However, in applications where high dose rate (> 1 krad/hr) is present, like in some high energy physics experiments, back channel leakage is still an issue.

It has been observed that the biasing condition on the gate of a transistor during irradiation affects the changes of threshold voltage and leakage current caused by the total dose. This is because that this bias voltage generates an electrical potential inside the gate oxide and that potential affects the transportation of hole-electron pairs generated by radiation which in turn affects the final trapped charges inside this gate oxide. The polarity and amount of the trapped charge are responsible for the radiation induced leakage current and for the threshold voltage change. With thin substrate, conductive back plate placed under or deposited on the substrate were used to provide bias and form a “back gate” after the irradiation to understand the mechanism of radiation induced back channel leakage [3] and to mitigate the leakage increase by applying a bias to back gate [5]. In reference [3], with a 150 micron sapphire substrate, 200 V bias has to be applied to the back plate in order to shift the I-V curve back to its pre-irradiation condition. In reference [5], Transistors fabricated using 0.15 micron SOI technology with buried oxide on silicon substrate are subjected to irradiation of a 70 MeV proton beam. Both leakage current increase and threshold voltage shift are observed in NMOS and in PMOS. Back gate bias is applied after the irradiation to move the I-V curve back to the pre-irradiation condition. The optimum value of the back gate voltage for both NMOS and PMOS is found to be -23 V.

I propose here a mechanism that is different from this back gate theory. I believe that by providing electrical potential in the substrate during irradiation when radiation induced hole-electron pairs are generated, transported, recombined and a few trapped, it is possible to affect the trapped charges in the substrate so as to control the leakage increase. In the back gate mechanism, because of the rather thick back gate insulation (the substrate thickness of a few hundreds of micro-meters comparing with the front gate oxide thickness of a few to a few tens of nano-meters), the required back gate bias is usually rather high to move the I-V curve after the irradiation. In the mechanism I propose, because it relies on guiding the transportation of different charges when they are

generated inside the substrate, the required bias should be much smaller than that in the back gate case. Take SOS CMOS as an example, radiation induced leakage current has been reported in NMOS, PMOS and in both transistors during irradiation tests at different dose rate and total dose. We know that trapped positive charge is responsible for leakage current in NMOS, while trapped negative charge is responsible for leakage in PMOS. If a bias is applied through the back plate to the substrate, positive bias will attract electrons towards the back plate leaving a higher positive charge density in part of the sapphire substrate that is close to the silicon-sapphire interface, hence causing leakage increase in NMOS and suppressing leakage in PMOS. When the bias voltage is negative, electrons are pushed toward the silicon-sapphire interface and that creates a higher negative charge density near the interface to cause leakage increase in PMOS while suppress the leakage in NMOS. An optimum bias voltage (constant or as a function of accumulated dose) may exist to have the minimum change in leakage and threshold voltage in both NMOS and PMOS. Tests have been carried out on one particular type of SOS device that is commercially available and the above predictions in leakage (or the lack of it) in NMOS and PMOS are confirmed. A constant optimum bias voltage for both NMOS and PMOS has been found to be only a few volts. Experiments are to be carried out to study this mechanism and its predictions on other types of SOI devices.

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