Total Ionization Dose Effect Studies of a 0.25 μm Silicon-On-Sapphire CMOS Technology

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35-word Abstract:
MOSFETs fabricated in a commercial 0.25μm Silicon-on-Sapphire CMOS technology are irradiated with a Co-60 gamma source followed by annealing studies at room temperature. New phenomena are observed and detailed data analyses are presented.

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I. INTRODUCTION

Silicon-on-Sapphire (SOS) CMOS technology has been a choice for radiation tolerant electronics since 1970. With the insulating sapphire substrate, this technology eliminates the parasitic bipolar junction transistors in the bulk silicon substrate and hence removes the mechanism for latch-ups. SOS technology has been reported to have smaller single event upset (SEU) cross sections than the bulk CMOS [1, 2]. However, like any Silicon-On-Insulator, SOS technology has back channel leakage under total ionization dose or TID effect [3, 4]. This back channel leakage is only controlled through special fabrication processes. In addition to the back channel leakage, there is edge leakage that is common to bulk CMOS and is usually mitigated through special layout techniques.

Historically, SOS technology was plagued by low-yield problems, thus it was limited to very specialized applications in military and space programs. Peregrine Semiconductor Corporation's Ultra Thin-Silicon-on-insulator (UltraCMOS) process overcomes this problem, making the SOS technology commercially available [5]. Previous tests showed that the 0.5 μm UltraCMOS process with special radiation hardening treatment can withstand radiation up to a few hundreds of krad (Si) [6].

Since Peregrine has introduced its 0.25 μm UltraCMOS process, we are exploring the applicability of this technology for the front-end readout ASICs in the optical link systems for the ATLAS [7] upgrade at the Large Hadron Collider [8].

To evaluate and characterize this new technology in radiation environment, we designed a test chip. The test chip was irradiated at 4 different dose rates for a total dose comparable to that in our application. Reported here are the results from the TID tests up to 100 krad.

II. THE SOS CMOS TEST CHIP AND EXPERIMENTAL SETUP

The basic features of the 0.25μm SOS CMOS technology used in the test chip are given in Table 1.

Table 1. The Technology features of the test chip

VDD	2.5V
Gate Oxide Thickness	6 nm
Process	0.25μm Silicon-on-Sapphire CMOS
Device isolation	LOCOS
Interconnectivity	3 metal layers
NMOS polysilicon gates doping	N+
PMOS polysilicon gates doping	P+

The test chip contains an 8×12 array of NMOS and PMOS transistors with different channel widths (80 and 40 μm) and lengths (0.25, 0.5, and 1.0 μm), implemented in four different types of layout: 4-finger, 8-finger, and 16-finger standard layout, and the enclosed-layout transistor (ELT). Since the edge leakage current is proportional to the number of edges in a transistor, the ELT and multi-finger transistors will help us understand the back channel and edge leakage currents. Each transistor of a particular size and layout has three identical copies. They are spread out in the transistor array for better measurement statistics. The test chip also contains ring oscillators, resistors, current mirrors, digital standard cells, and shift registers for SEE characterization. Tests on these structures are discussed elsewhere.

The I-V characteristic curve of each transistor is measured using a picoammeter (Keithley Model 6485) and three programmable DC power supplies. A reed relay switch array controlled

by a USB DIO card is used to connect the terminals of the transistor under measurement to the picoammeter and the DC power supplies. I_D is measured as a function of V_{GS} before and after the radiation while V_{DS} is fixed at 0.1V for NMOS and –0.1V for PMOS. The V_{GS} sweeps from 0 to 1.5V when measuring NMOS transistors and from -1.5 to 0 V in the PMOS case. During irradiation the NMOS transistors are biased with V_{DS} = 2.5 V, the PMOS with V_{DS} = -2.5 V.

III. MEASUREMENT RESULTS AND DISCUSSION

Shown in Fig. 1 are the I-V curves of NMOS and PMOS transistors (W/L = 40/0.25 um, ELT) before and immediately after the irradiation at 4 different total doses with the same dose rate of 1.2 krad/hr. As seen in Fig. 1, at a low dose (7.6 and 33 krad(Si)), the I-V curves of the NMOS transistors shift left (Vt decreases) as the leakage current increases. At a high dose, the I-V curves shift right (Vt increases) without an increase in leakage current. In contrast to the NMOS case, the I-V curves of PMOS transistors (W/L = 40/0.25um, ELT) stay unchanged at the low dose (≤ 33 krad (Si)) but move left (|Vt| decreases) at high dose (86 krad (Si)) with an increase in leakage current. This observation indicates that the net trapped charge is positive at low dose and becomes negative at high dose. Leakage current vanishes in both cases after a proper period of annealing at room temperature.

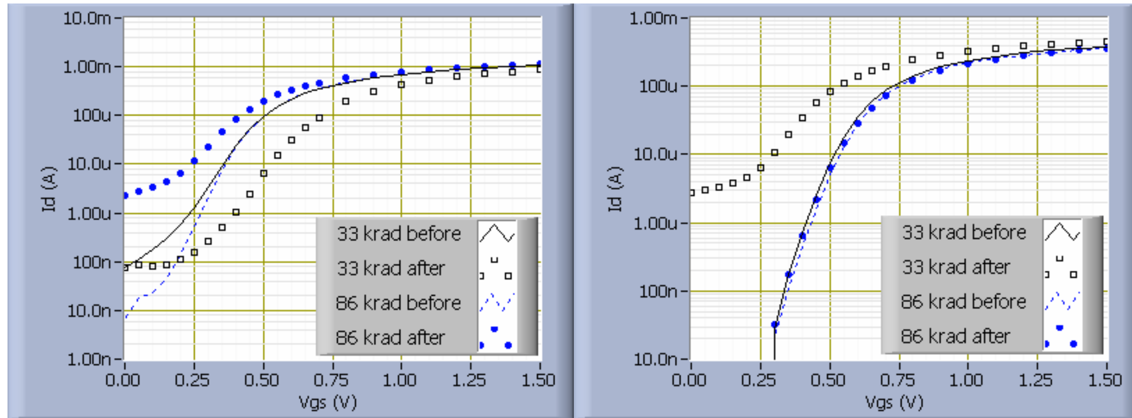

Fig. 1. The I-V curves of NMOS (left) and PMOS (right) ELT transistors

In general, An increase in leakage current can be attributed to the radiation induced charge accumulation in three places: the gate oxide, the field oxide (edge) and the sapphire substrate. The data shows that using enclosed layout technique effectively limits edge leakage. In order to estimate the increase in gate leakage current, which is correlated to threshold voltage shift, we shift the pre-irradiation ELT I-V curve by ΔV, the change on Vt caused by the irradiation. We found that the corresponding current increase is very small in both NMOS and PMOS cases and is within our measurement error. From this we conclude that the increase in leakage current has a large component that is not correlated to the threshold voltage shift and that the radiation induced gate leakage is small.

Shown in Fig. 2 is a study on the edge and back channel leakage currents. Leakage current in ELT and in standard transistors of 16 fingers were compared for NMOS. All the transistors have the same width (40 um) and length (0.25 um) and were irradiated at 1.2 krad/hr. In the ELT case, the dominating source for leakage current is the back channel. In the case of a standard layout transistors, the leakage current has two contributions: the edge and back channel. In Fig. 2, it is shown that the leakage current in standard layout transistors is higher than that in an ELT. This indicates that the back channel leakage is a large contribution in the increase of total leakage

current in both NMOS and PMOS. Since the edge leakage adds to the total leakage on top of the back channel, this indicates that the trapped charge in the field oxide and in the sapphire have the same sign. In NMOS, the net trapped charge in both the edge field oxide and the sapphire are positive at low dose, causing parasitic conducting channels at the side (edge) of the gate and back of the transistor body. The leakage current returns to before-radiation level after radiation reaches a total dose above 33 krad (Si). In PMOS, the leakage current increase is only present at high dose. Since trapped charge in the edge field oxide and in the sapphire is the same in both NMOS and PMOS cases, we believe that there are competing processes that result in the net trapped charge to be positive at low dose but become negative at high dose. This contributes to the increase in leakage current at low dose for NMOS but at high dose for PMOS. This result is new compared to what have been reported in literature. In [3, 4], trapped positive charge is believed to induce leakage current in NMOS, but not in PMOS. In [9] trapped negative charge is believed to induce the leakage in PMOS, but not in NMOS.

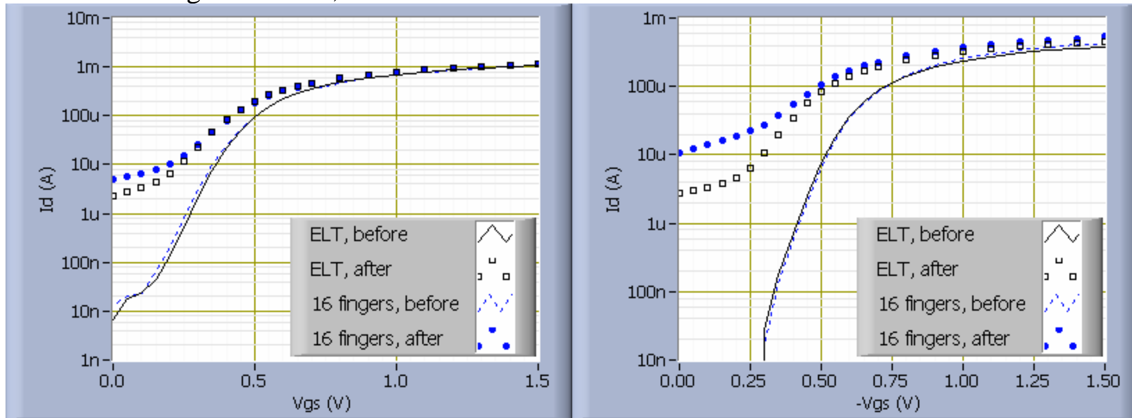

Fig. 2 The layout effect on NMOS (left) and PMOS (right) transistors

Shown in Fig. 3 are the leakage current and threshold voltage change with respect to those before irradiation of the NMOS (left) and the PMOS (right) transistors in the annealing study.

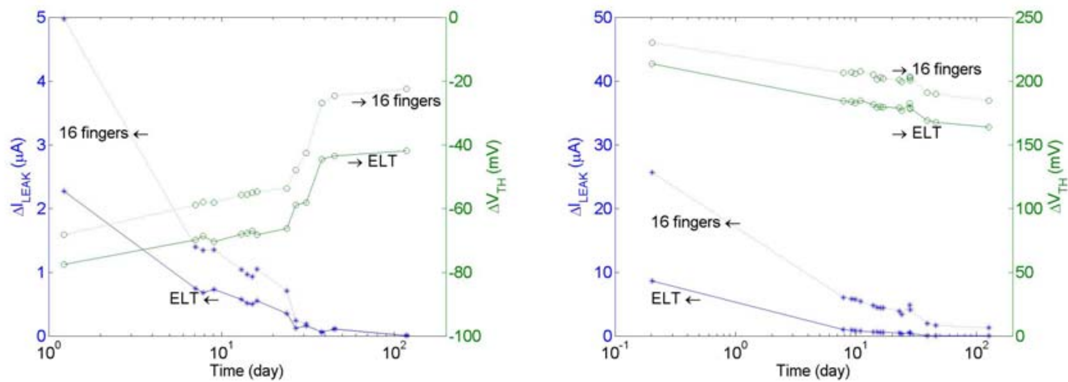

Fig. 3.The anneal of NMOS (left) and PMOS (right) transistors

The transistors (W/L = 40/0.25, ELT layout and 16 finger standard layout) are irradiated to 33 krad (Si) at 1.2 krad/hour for the NMOS, 100 krad (Si) at 30 krad/hour for the PMOS. As seen in this figure, in both NMOS and PMOS cases, almost all the increased leakage current anneals back to zero, indicating that leakage current would not be a problem in realistic dose rate in our applications. The threshold voltage shift is not large in NMOS and a big fraction of that anneals back. In the PMOS case, the shifted threshold voltage anneals a small part in 120 days. The

annealing process is roughly linear with a logarithmic time axis, indicating that the dominating annealing process follows the tunneling annealing model [10]. Since the annealing process continues with time, we do not observe significant permanently trapped charge both in the field oxide and in the sapphire. This also indicates that net trapped charge does not come from the interface trap at the sapphire interface [11].

IV. CONCLUSION

MOSFETs fabricated in a commercial 0.25 μm Silicon-on-Sapphire technology are irradiated with a Co-60 gamma source up to 100 krad(Si). An increase in leakage current is observed after irradiation in NMOS only at low dose and in PMOS only at high dose. The increase in leakage current is due to the net trapped charge polarity change with the increase of total dose. This leakage current increase anneals almost back to zero at room temperature and the annealing roughly follows the tunneling model. No significant permanently trapped charge is found. This technology is qualified for ASIC development in our applications in high energy physics experiment.

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