Design Techniques for Radiation-Hard Phase-Locked Loop Components in a 0.25μm SOS CMOS Process

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35-word Abstract:
This paper describes the design techniques of several key building blocks of a radiation-hard Phase-Locked Loop (PLL), fabricated in a 0.25um SOS CMOS process. The irradiation testing results of all the PLL components are also provided.

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I. INTRODUCTION

Phase-locked loops (PLLs) are widely used as frequency multipliers in many analog and mixed-signal applications. In this paper, we present the design techniques and irradiation test results of several key building blocks of a radiation-hard PLL. These components include a voltage controlled oscillator (VCO) with a frequency range from 2.6GHz to 3.5GHz, a 3.5GHz current mode logic (CML) divider and a phase-frequency detector (PFD). The circuits are designed and implemented using Peregrine's 0.25µm Silicon-on-Sapphire (SOS) CMOS process. The comparison between the pre- and post-radiation test results shows that all the components are radiation-hard after a 100Krad of proton irradiation.

II. SILICON-ON-SAPPHIRE CMOS TECHNOLOGY

We chose to use Peregrine's 0.25µm SOS CMOS process in our design for its better SEE immunity than bulk CMOS [1, 2]. However, the total ionization dose effects in SOS may be of a concern because of the back channel leakage [3, 4]. We performed a total ionization irradiation test using gamma source of 100Krad on several test structures. We found that the threshold voltage V_{tn} of NMOS devices increases by about 0.2V whereas the absolute value of the threshold voltage of PMOS devices, $|V_{tp}|$, decreases by about 0.17V [5]. The increased leakage current in both devices becomes negligible after annealing, but the threshold voltage shift remains. The results are shown in Fig.1

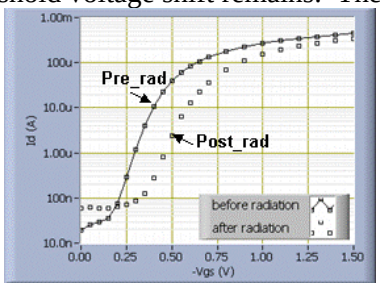

Figure 1(a). Pre- and Post-rad Ids-Vgs curves for NMOS

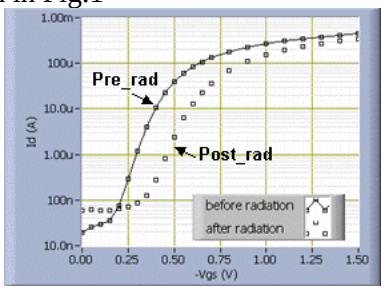

Figure 1(b). Pre- and Post-rad Ids-Vgs curves for PMOS

III. PHASE-LOCKED LOOP DESIGN

A typical PLL is a feed-back system, consisting of a PFD, a VCO, a divider, a charge pump and a loop filter, as shown in Fig.2. The loop filter typically uses passive components; therefore it is generally considered radiation hard. However, the PFD, the VCO and the divider, are sensitive to radiation-induced effects such as threshold voltage variations. If not carefully designed, the performance of these PLL components may degrade significantly after irradiation and the PLL may not lock. In this section, we describe our rad-hard PLL design techniques.

A. Voltage Controlled Oscillator

One of the most important design specifications for a VCO is its frequency versus control voltage characteristic. If this characteristic changes due to radiation, it will affect the central frequency of the VCO as well as its tuning range, resulting in an unstable PLL. Therefore, it is desirable to have a VCO of which the frequency remains unchanged at a given a control voltage in the presence of radiation. With such goal in mind, we designed a differential delay cell with symmetrical load [6] as the building block of our VCO, based on the irradiation results of the PMOS and NMOS devices in the SOS CMOS technology.

The delay cell consists of an NMOS differential pair, an NMOS tail current source, and two PMOS symmetrical loads as shown in Fig. 3. The symmetrical load presents a near-resistive characteristic and at the same time is adjustable by a control voltage. We designed the delay cell so that the delay remains almost constant even with radiation-induced variations on V_{tn} and $|V_{tp}|$ for a given control voltage. In our VCO delay cell design, the delay is determined by the time it takes to charge and discharge the

capacitance at the output node through the PMOS load and the NMOS differential pair and the tail current source. The delay of each delay stage can be written as:

$$T_d = T_r + T_f$$

Where $T_r = R_p C$, $R_p = 1/g_{mp} = 1/\left[k_p {}^{W}\!/_{L} (V_{sgp} - |V_{tp}|)\right]$

Therefore, $T_r \propto 1/(V_{sgp} - |V_{tp}|)$ (1)

And on the other hand, $T_f = (C\Delta V)/I_n \propto 1/(V_{gsn} - |V_{tn}|)^2$ (2)

We can see from equations (1) and (2) that T_r increases as $|V_{tp}|$ increases and similarly T_f increases as $|V_{tn}|$ increases. As mentioned in section II, for the SOS technology we use, radiation causes V_{tn} to increase and $|V_{tp}|$ to decrease, resulting in an increased T_r and a decreased T_f. Therefore, if we design the VCO in such a way that the changes of these two factors, T_r, and T_f, are comparable to each other, they will cancel each other out and the total cell delay T_d remains constant. This will result in a very robust VCO design which is insensitive to the irradiation-induced variations. Our VCO consists of four stages of differential delay cells and it is designed to have a tuning range from 2.35GHz to 2.9GHz. The irradiation test result (section IV) shows that this VCO design is insensitive to the irradiation-induced variations.

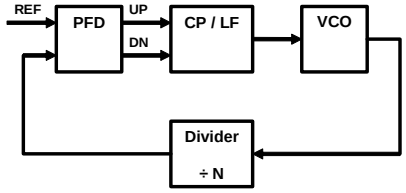

Figure 2. Basic structure of a PLL

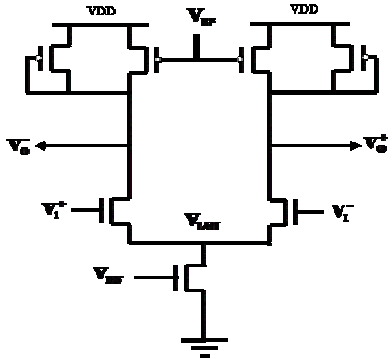

Figure 3. A fully differential delay cell with symmetric load

B. Current-Mode-Logic Divider

The divider needs to work at least for the same frequency range of the VCO output. There are two challenges in the divider design: a) how to operate it at multi-GHz range and b) how to make it robust in the presence of radiation. We designed a current-mode-logic (CML) divider [7, 8] to meet the two challenges. The schematic of the divider is shown in Fig. 4. It is composed of two latches: a master latch and slave latch. The feedback from the output of the slave latch to the input of the master latch performs the divide-by-2 function. Depending on the input signals from the VCO outputs (clk and clkb), transistors m1-m8 will be turned-on or off, generating the corresponding outputs. Due to the current steering feature of this design, the circuit can work at very high speed. In addition, the tail current in current-mode logic design remains constant because the two transistors in the current mirror both experience the same V_t shift. The post layout simulation shows that the divider can work up to 3.5GHz. For testing purpose, we have 4 stages of the CML dividers cascaded together to divide the VCO output frequency down by 16.

C. Phase-Frequency Detector

A PFD is used to compare the phase between two signals, the reference clock and the feedback clock, and generate the “up” and “down” control signals based on the phase difference between those two. We chose a PFD design which consists of two DFFs and an AND gate, as shown in Fig. 5. When the reference clock leads the feedback clock, the PFD will generate an “up” signal corresponding to their phase difference; vice versa, when the feedback clock leads the reference clock, the PFD will generate a proportional “down” signal.

Both DFF and NAND gates in the PFD are CMOS digital circuits. To take into consideration of the radiation effects in the design, we incorporated the V_{tn} and $|V_{tp}|$ shift due to irradiation into the SPICE models to simulate the circuits. Simulation results show that the PFD can work up to 250MHz.

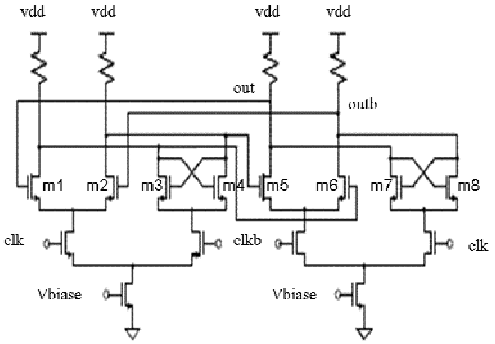

Figure 4. Schematic of the CML Divider

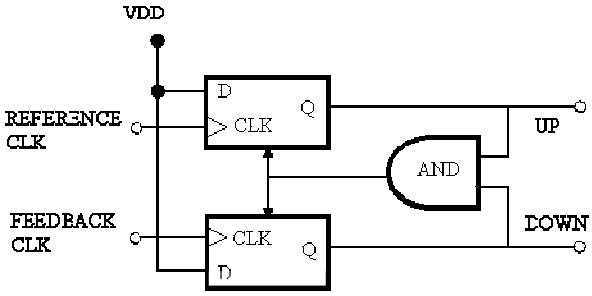

Figure 5. Schematic of the PFD

IV. RADIATION TEST RESULTS

The PLL components were first tested in the lab and were then exposed to a 230MeV proton beam up to 100Krad with a flux of 1 x 10^7 proton/cm^2/s.The pre- and post-measurement results of each component are described as following.

A. VCO measurement results

Figure 6 shows the pre- and post measurement results as well as the simulation result of the VCO's frequency versus control voltage characteristic. As can be seen, the pre- and post-rad results match almost perfectly (within 4%). This verifies the radiation hardness of our VCO design.

The signal amplitude of the VCO output has some small variations after irradiation as shown in Fig. 7. This is due to the variation in the NMOS tail current caused by V_{tn} shift. This variation is small so it does not affect the operation of the CML divider.

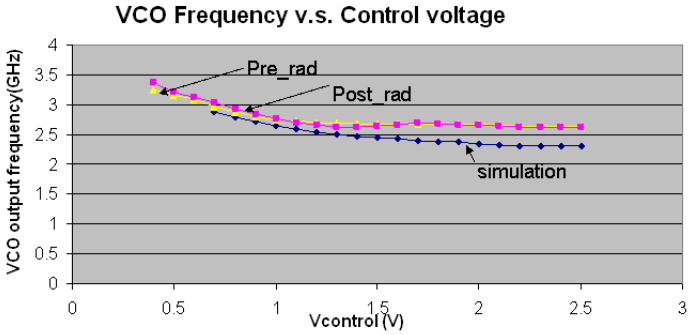

Figure 6. Simulated and Measured (Pre- and Post-rad) VCO output frequency v.s. control voltage

The VCO jitter was also measured as shown in Fig. 8. Pre- and post-rad results show that irradiation introduces about additional 3ps jitter on the VCO output.

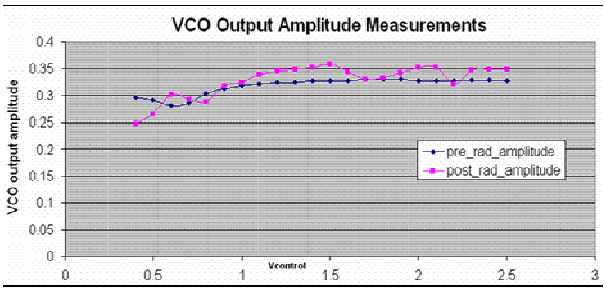

Figure 7. The measured VCO output amplitude.

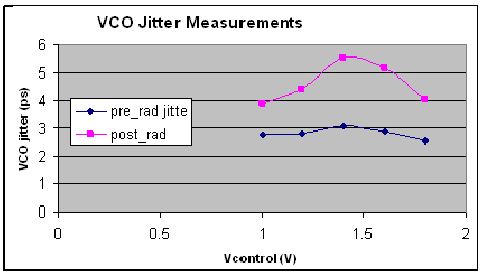

Figure 8. The measured VCO jitter.

B. CML Divider

The CML divider was tested up to 2.75GHz (limited by the test equipment) with 50% duty cycle inputs (clk and clkb). The post-rad results show that the divider works at the same speed as in pre-rad, with only a slight reduction on the output amplitude (shown in Fig. 9 (a) and (b)).

C. PFD

Different combinations of reference clock and feedback clock were applied to the PFD to test its functionality and performance. We observed literally no difference between the pre-rad and post-rad measurement results. In Figure 10 is shown the measured pre- and post-rad PFD output ("up" signal) when both refclk and feedback clock are at 250MHz but one is leading the other by 2ns in phase. The PFD generates the "up" output pulse of 2ns. The measured pre- and post-rad PFD outputs are almost identical.

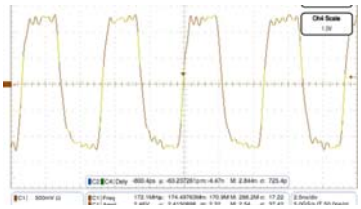

Fig. 9 (a) measured CML divider output (pre-rad) at 2.75GHz.

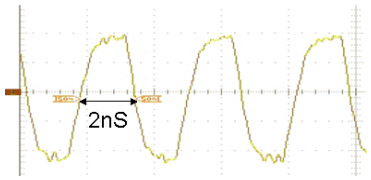

Fig. 10 (a) measured PFD output (pre-rad)

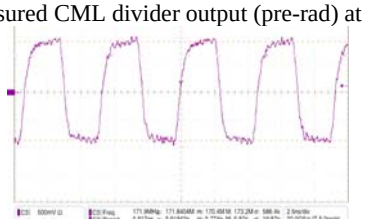

Fig.9 (b) measured CML divider output (post-rad) at 2.75GHz.

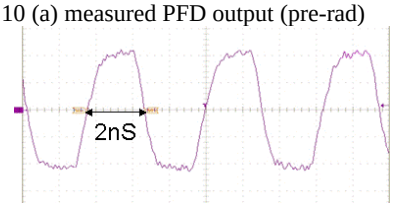

Fig. 10 (b) measured PFD output (post-rad)

V. CONCLUSION

We presented design techniques of several key building blocks of a radiation-hard phase locked loop, including a VCO with tuning frequency from 2.6 to 3.5GHz, a 3.5GHz CML divider and a PFD, and the irradiation results of these circuits with proton beam source of 100Krad. The comparison between the pre-rad and post-rad results shows that the PLL circuits are robust and insensitive to radiation-induced variations.

VI. ACKNOWLEDEMENTS

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