Design, Analysis and Total Ionization Dose Test of a 3GHz Voltage-Controlled-Oscillator

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I. INTRODUCTION

Voltage Control Oscillator (VCO) is one of the most sensitive components in Phase-locked loops (PLLs). This paper presents the design, analysis and total ionization dose (TID) measurement results of a 3GHz VCO designed and implemented using a commercial 0.25µm Silicon-on-Sapphire (SOS) CMOS process. First, we present the TID effects on single NMOS and PMOS transistors made in a test chip using the same technology. We then present the theoretical analysis of a VCO design using symmetrical load. This is followed by simulations of radiation effects on various VCO performances such as tuning range and phase noise. In the end, we present the TID measurement results of the VCO with up to 100Krad of Proton irradiation that support our analysis.

II. SILICON-ON-SAPPHIRE (SOS) CMOS TECHNOLOGY

We chose Peregrine's 0.25µm Silicon-on-Sapphire CMOS (UltraCMOS®) process for its improved SEE immunity than bulk CMOS [1, 2]. But the total ionization dose effect (TID) in SOS may be a concern because of its back channel leakage [3, 4]. We did a total ionization irradiation test using gamma source of 100Krad on several test structures made using this process and found that:

1) Leakage current will increase in both NMOS and PMOS devices due to irradiation but the leakage current in both devices become negligible after annealing. Therefore the leakage current will not be a concern for our application.
2) Threshold voltages Vtn and Vtp both change after irradiation and remain about the same after annealing. The results are shown in Fig.1. The Vtn of NMOS devices increases by about 0.2V whereas the |Vtp| (the absolute value of Vtp) of PMOS devices decreases by about 0.17V [5]. As we know, the threshold voltage variations can affect the VCO performances such as VCO start-up behavior, tuning range, phase noise, and output swing, etc. Therefore it is very important to analyze and understand the VCO behavior with Vtn and |Vtp| variations in order to design a robust VCO.

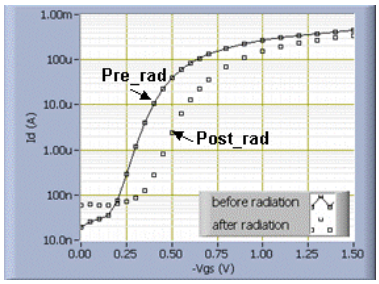


Figure 1(a). Pre- and Post-rad Ids-Vgs curves for NMOS devices. Vtn increases by 0.2V from 0.44V.

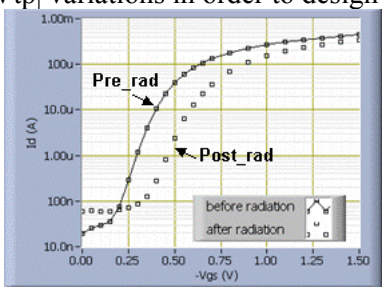
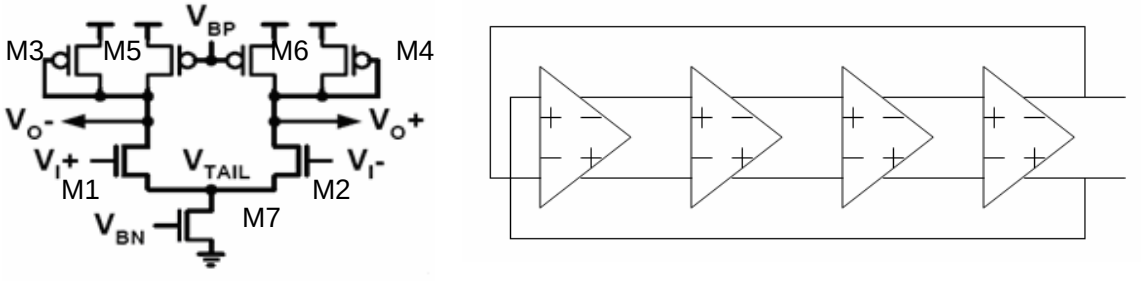


Figure 1(b). Pre- and Post-rad Ids-Vgs curves for PMOS devices. |Vtp| increases by 0.17V from 0.4V.

III. THE DESIGN AND ANALYSIS OF A VCO WITH SYMMETRIC LOAD

A. Voltage Controlled Oscillator (VCO) with symmetric load

We designed a differential delay cell with symmetric load as the building block of our VCO. The delay cell consists of an NMOS differential pair, an NMOS tail current source, and a PMOS symmetrical load as shown in Fig. 2 (a). The VCO is composed of 4 stages delay cells as shown in Fig. 2 (b).



(a) (b)

Fig. 2 (a) The VCO delay cell. (b) A four-stages VCO.

The buffer delay can be defined as: $t = R_{EFT} \cdot C_{EFT}$ (1)

where R_{EFT} is the VCO output resistance and C_{EFT} is the total output capacitance between every stage.

When the control voltage Vbp changes from GND to VDD, R_{EFT} changes according to the working mode (regions) of transistors M5 and M3: linear, saturation or cut-off.

When V_{BP} increases from GND up to $V_O - |V_{TP}|$, M5 works in linear mode and M3 in saturation mode. Most of the tail current goes into M5 because of the large Vsg across M5 and a smaller Vgs3 across M3. The current through M5 can be expressed by following formula:

$$I_{SD} = k_{m5} \cdot [(V_{SG} - |V_{TP}|) \cdot V_{SD} - \frac{V_{SD}^2}{2}] \cong k_{m5} \cdot (V_{SG} - |V_{TP}|) \cdot V_{SD} \quad (2)$$

Therefore the output resistance of M5 can be approximated as the following:

$$r_{m5} = \frac{\partial V_{SD}}{\partial I_{SD}} = 1 \Big/ k_{m5} \cdot (VDD - V_{BP} - |V_{TP}|) \quad (3)$$

The transconductance of transistor M5, g_{m5} (the tail current) can be expressed by another formula:

$$g_{m5} = k_{m5} \cdot (V_{SG} - |V_{TH,P}|) = \frac{I_{SD}}{V_{SD}} = \frac{k_{m7}}{4 \cdot V_{SD}} (V_{BN} - V_{TH,N})^2 \quad (4)$$

Since large portion of the tail current flows into M5 and only a small potion goes to M3, g_{m3} is small, and 1/gm3, which is equivalent resistance of M3 is large. Therefore r_{m5} dominates the overall R_{EFT}. So the frequency for the N stages delay cell can be given by:

$$F = k_{m5} \Big/ N \cdot C_{EFT} \cdot (VDD - V_{BP} - |V_{TP}|) \quad (5)$$

Or

$$F = k_{m7} \Big/ 4N \cdot C_{EFT} \cdot V_{SD} \cdot (V_{BN} - V_{TN})^2 \quad (6)$$

As can be seen from equation (4), the VCO output frequency is inversely proportional to the VCO control voltage V_{BP}. We call this region the "linear region".

When V_{BP} continues to increase so that $V_O - |V_{TP}| \le V_{BP} \le$ VDD- $|V_{TP}|$, M5 enters into saturation region. The total output resistance R_{EFT} is the parallel combination of r_m5 and $1/g_{m3}$. Since M5 is in now saturation region, r_{m5} is the output resistance of a current source M5, which is larger, compared to $1/g_{m3}$. Therefore the overall resistance R_{EFT} is dominated by $1/g_{m3}$. We know that

$$g_{m3} = k_{m3} \cdot (V_{BP} - V_T) = \sqrt{2 \cdot k_{m3} \cdot I_{D3}} \tag{7}$$

$$I_{d3} = \frac{I_{tail}}{2} - I_{D5} = \frac{1}{4} \cdot k_{m7} \cdot (V_{BN} - V_{TN})^2 - \frac{1}{2} \cdot k_{m5} \cdot (VDD - V_{BP} - |V_{TP}|)^2 \tag{8}$$

So the frequency for the N stages delay cell can be given by:

$$\mathrm{F} = \frac{\sqrt{2 \cdot k_{m3}}}{N \cdot C_B} \cdot \left(\sqrt{\frac{1}{4} \cdot k_{m7} \cdot (V_{BN} - V_{TN})^2 - \frac{1}{2} \cdot k_{m5} \cdot (VDD - V_{BP} - |V_{TP}|)^2}\right) \tag{9}$$

In this case, the VCO output frequency is proportional to the VCO control voltage V_{BP}.
We call this region the "saturation region".

When V_{BP} increases even further to $V_O - |V_{TP,P}| \le V_{BP} \le VDD$, M5 enters into cut-off mode and the total output resistance can be roughly expressed by $1/g_{m3}$:

where $$g_{m3} = k_{m3} \cdot (V_{BP} - V_T) = \sqrt{2 \cdot k_{m3} \cdot I_{D3}} \tag{10}$$

$$I_{d3} = \frac{I_{tail}}{2} = \frac{1}{4} \cdot k_{m7} \cdot (V_{BN} - V_{TN})^2 \tag{11}$$

So the frequency for the N stages delay cell becomes:

$$\mathrm{F} = \frac{\sqrt{k_{m7} \cdot k_{m3}}}{\sqrt{2} \cdot N \cdot C_B} \cdot (V_{BN} - V_{TN}) \tag{12}$$

The VCO output frequency when M5 is in the cutoff region becomes independent of V_{BP}. We call this region as "cutoff region".

Figure 3 shows the simulation of Frequency v.s. Control voltage Vbp over the three regions as Vbp changes from 0V to 2.5V.

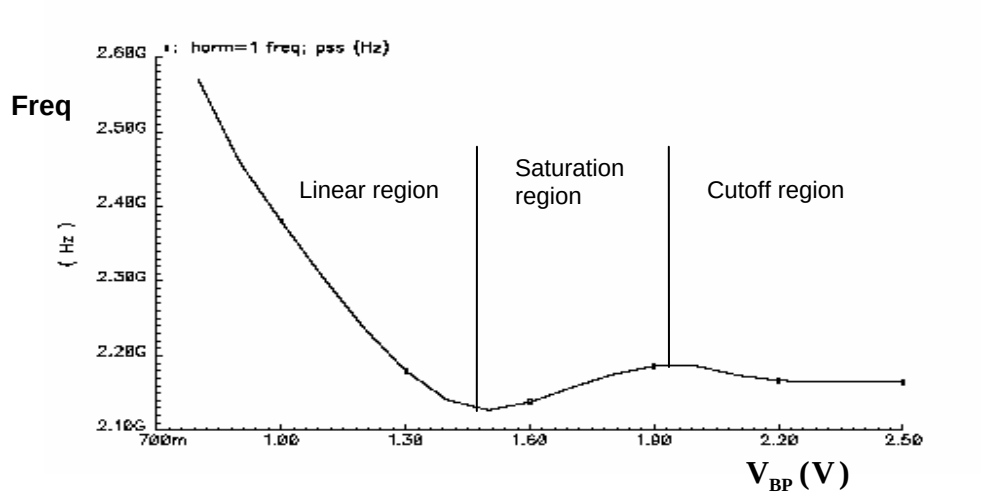


Fig.3 VCO output frequency range versus VCO control voltage V_{BP} at V_{BN}=0.7V

B. Tuning Range

The change in Vtn and |Vtp| will change VCO tuning range. In the linear region, the decrease in |Vtp| will cause the VCO output frequency to increase according to equation (5). In the saturation region, the increase in Vtn and decrease in |Vtp| will decrease output frequency according to equation (9). In the cutoff region, the output frequency will not change with the VCO control voltage V_{BP} but the VCO output frequency will decrease as Vtn increases, according to equation (12).

The simulation results in Fig.4 (a) show the VCO tuning range versus V_{BP} with different scenarios of Vtn and |Vtp| with V_{BN} =0.7V. Under each scenario, transistors M3/M4 experiences three different regions:

linear, saturation and cutoff region as predicted the analysis above, while M5/M6 are in saturation or cut off region depending on the output swing. In the linear region, the VCO output frequency increases as Vtn increases and |Vtp| decreases where as in saturation and cutoff region, the VCO output frequency decreases. This is consistent with our analysis above.

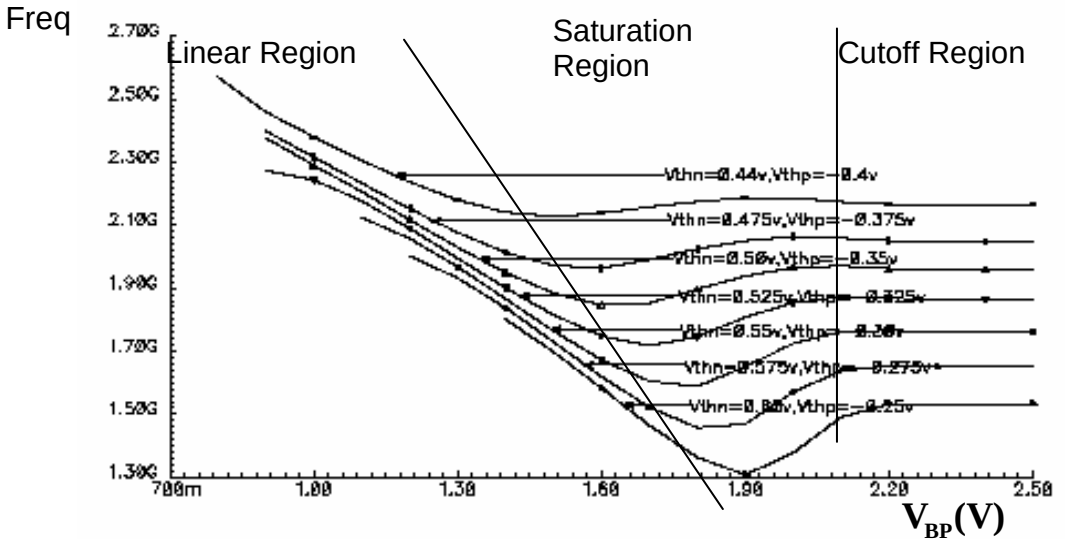


Fig.4 (a) VCO tuning range with variations in Vtn and |Vtp| at V_{BN}=0.7V

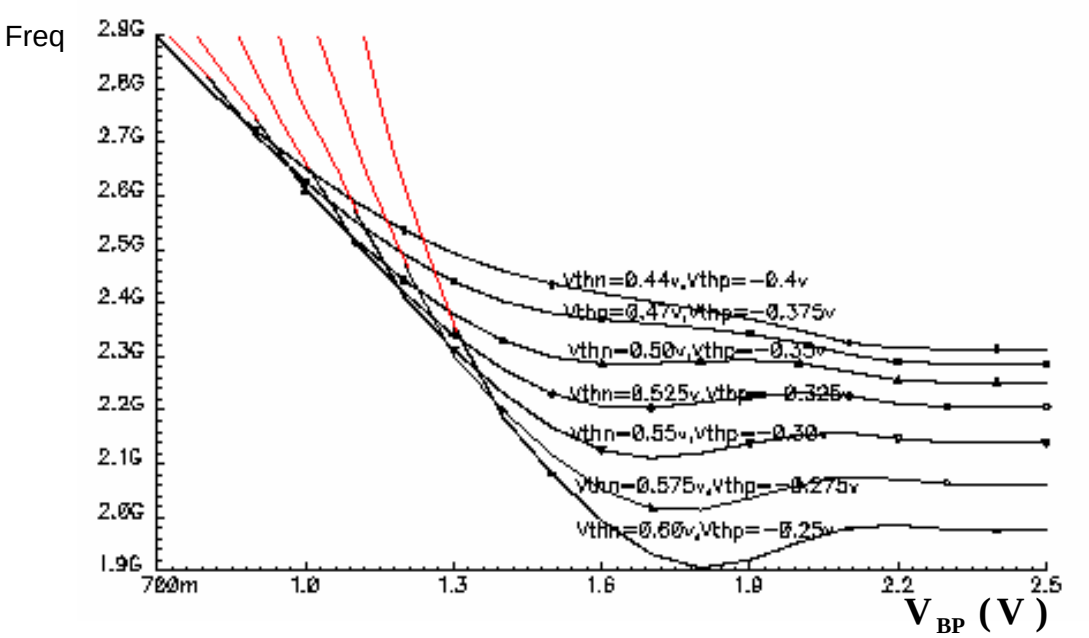


Fig.4 (b) VCO tuning range with variations in Vtn and |Vtp| at V_{BN}=0.8V

The simulation results in Fig.4 (b) show the VCO tuning range versus the VCO control voltage V_{BP} with different scenarios of Vtn and |Vtp| and V_{BN} =0.8V. From equations (5), (9) and (12) we see that increasing bias voltage V_{BN} will increase VCO output frequency in linear region more than in the saturation and cutoff region. This makes the Frequency v.s. control voltage curve monotonic, shown as the top curve in Fig.4 (b). Also from Fig.4 (a) and (b), we see that the variations of Vtn and |Vtp| may make the Frequency v.s. Vbp non-monotonic even with V_{BN} =0.8V.

C. Radiation Effects on VCO Start-Up Condition

According to the "Barkhausen criteria", the minimum gain A_0 for the delay cell in a 4-stage ring oscillator should be:

$$A_0 = g_{m1,2} \cdot r_{m5} = g_{m1,2} \Big/ k_{m5} \cdot (VDD - V_{BP} - |V_{TH,P}|) \tag{13}$$

when M5 is in linear region.

$$A_0 = g_{m1,2} \cdot R_{out} \cong g_{m1,2} / g_{m5,6} \geq \sqrt{2} \tag{14}$$

when M5 is in saturation region.

The increase in Vtn will cause the transconductance of NMOS devices M1 and M2 $g_{m1,2}$ to decrease. Likewise, the decrease in |Vtp| will cause $g_{m5,6}$ to increase, causing delay cell gain A_0 to decrease in the equation (13) and (14). The simulation results in Fig.4 (a) and (b) confirms this, showing that with an increased Vtn and decreased |Vtp|, the VCO start-up to oscillate at higher VCO control voltage V_{BN} than in the pre-rad case.

D. Voltage Controlled Oscillator Phase Noise

The total noise current in the VCO are determined by the differential transistors and symmetrical loads [9]. The symmetrical load is composed of two PMOS transistors: one in diode connection and the other controlled by the VCO control voltage Vbp. The total noise current of each of output nodes can be expressed by [9]:

$$\frac{\bar{i_n^2}}{\Delta f} = \left(\frac{\bar{i_n^2}}{\Delta f}\right)_N + \left(\frac{\bar{i_n^2}}{\Delta f}\right)_{p\_sat} + \left(\frac{\bar{i_n^2}}{\Delta f}\right)_{p\_ctrl} = \frac{4KTI_{tail}}{V_{char}} + 4KT\gamma \cdot g_{mp\_sat} + 4KT\gamma \cdot g_{mp\_ctrl} \tag{15}$$

Where $V_{char}=(V_{gs}-V_{th})/\eta$ in the long channel devices.

Hence the VCO has the phase noise:

$$L_{\min}\{\Delta f\} = \frac{8}{3\eta} \cdot \frac{KT}{I_{tail}} \cdot \left(\frac{\eta}{V_{gs} - V_{tn}} + \frac{\gamma \cdot g_{m3}}{I_{tail}} + \frac{\gamma \cdot g_{m5}}{I_{tail}}\right) \cdot \frac{f_0^2}{\Delta f^2}, \tag{16}$$

Formula (16) shows that three parts contribute to the phase noise: a) input differential transistor; b) the diode-connected PMOS transistor in the symmetrical load; and c) the PMOS transistor controlled by V_{BP} in the symmetrical load.

An increase in Vtn will cause the first item in formula (16) to increase. A decrease in |Vtp| will cause the second and the third items to also increase, due to the increased transconductance of PMOS in the symmetrical load. In particular, for the third term, the transistor M5 can work at three different regions: linear, cut off or saturation region. Since transistor in saturation region has larger transconductance than that in linear or cut-off region, M5 in saturation region generates more noise. Therefore from the phase noise viewpoint, we prefer that M5 works in the linear region [10].

In addition, an increase in Vtn will cause the tail current source (made of M7) to have less current, which will further increase the total VCO phase noise according to formula (16). Fig.5 illustrates the effects of Vtn and |Vtp| variation on VCO phase noise.

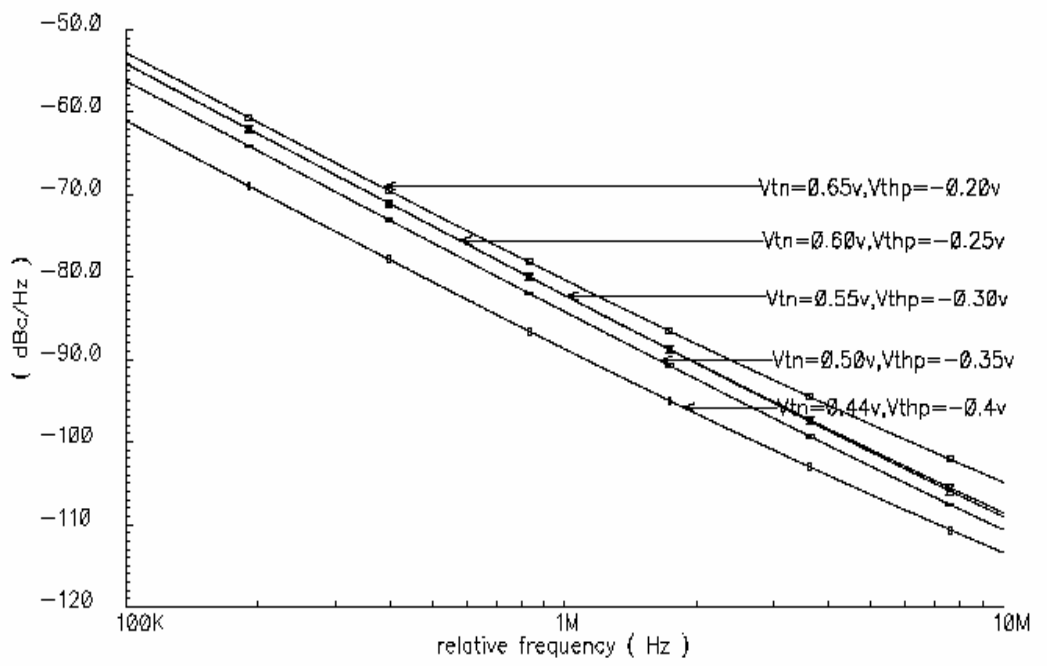


Fig.5 the VCO phase noise simulation results when transistors threshold voltage changing

In summery, with an increase in Vtn and decrease in |Vtp|, the VCO phase noise will increase. This suggests that a VCO with PMOS as differential transistors and NMOS transistors as a symmetrical load can improve phase noise performance, but at the price of a reduced VCO speed.

IV. RADIATION TEST RESULTS

The VCO components were fabricated using Peregrine's 0.25um SOS CMOS technology and the layout of the VCO is shown in Fig. 6.

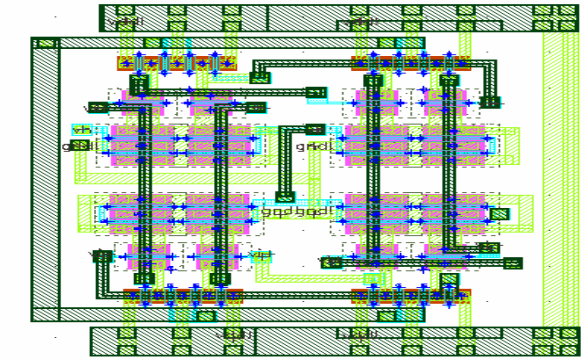
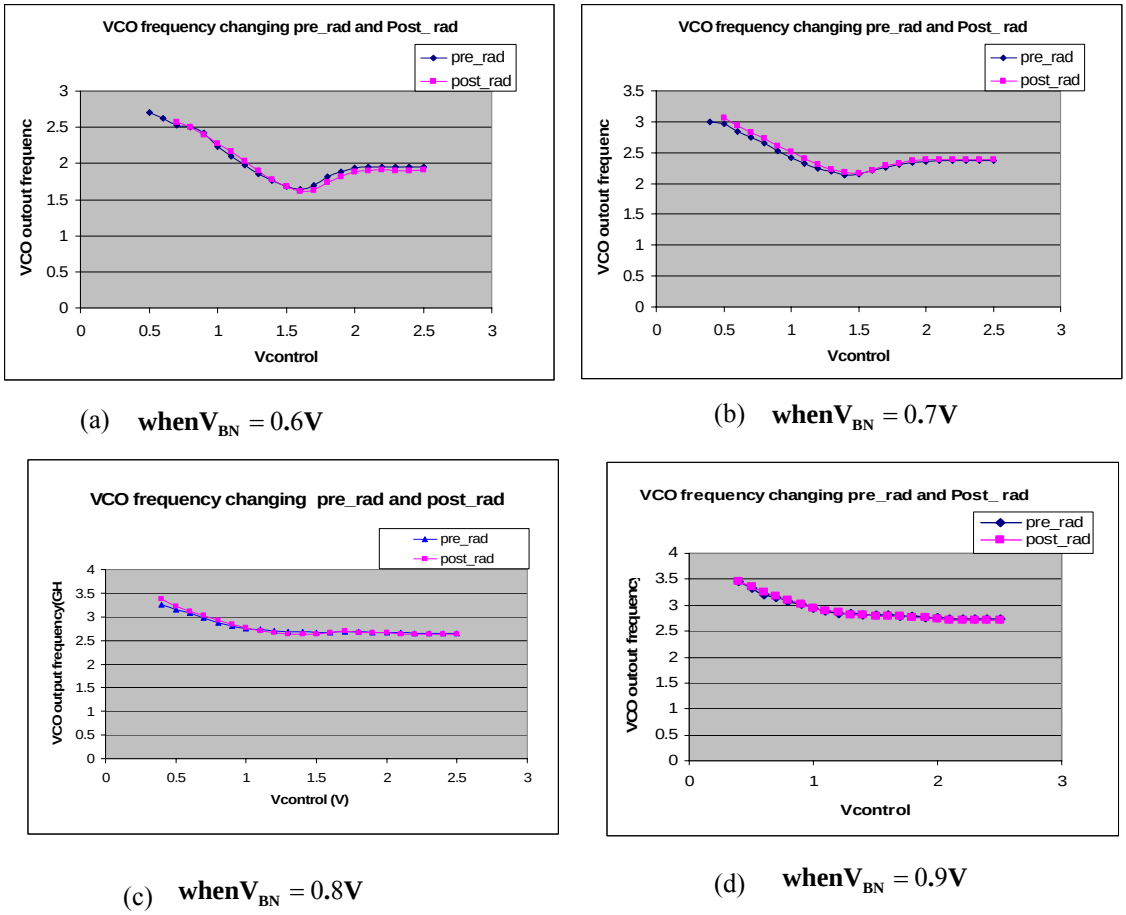


Fig.6: the layout of a four-stages differential ring VCO with symmetric load.

The VCO performances were tested in lab and then exposed to a 230MeV proton beam up to 100Krad with a flux of 1 x 10^7 proton/cm^2/s. The pre- and post-measurement results are shown below.

A. VCO tuning range measurement results

Figure 7 shows the VCO output frequency versus VCO control voltage when biasing control voltage V_{BN} changes from 0.6v to 0.9v.



(a) **whenV_{BN} = 0.6V**

(b) **whenV_{BN} = 0.7V**

(c) **whenV_{BN} = 0.8V**

(d) **whenV_{BN} = 0.9V**

Fig.7 VCO output frequency versus Vbp when biasing control voltage V_{BN} changes from 0.6v to 0.9v

From Fig. 7, we can make the following observations.

a) The VCO experiences three different regions: linear, saturation and cutoff region as V_{BN} increases, consistent with out analysis. When VCO bias voltage V_{BN} increases, it can make the Frequency v.s. Vbp curve monotonic (shown in Fig.7 (c), (d)).

b) The increase in Vtn and decrease in |Vtp| increases the VCO frequency in linear region and decrease VCO frequency saturation and cutoff region, consistent with formulas (5), (9) and (12).

c) The increase in Vtn and decrease in |Vtp| causes the VCO to start to oscillate at higher Vbp compared to the pre-rad case.

B. VCO jitter measurement results

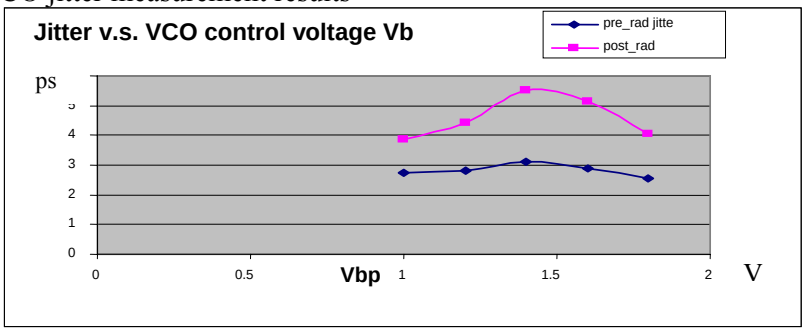


Fig.8 Pre-rad and post-rad VCO jitter measurement over three working regions. (Vbn=0.8V).

The VCO jitter is measured and shown in Fig.8. The post-rad jitter is measured to be larger than that of pre-rad, in compliance with out analysis. Also we can see that the VCO have a larger jitter when the PMOS load works in the saturation region than in the linear region. This again confirms our analysis. Therefore form the view point of noise, we prefer the VCO working in the linear region [10].

In summary, all test results are consistent with our analysis and simulation results. Some minor differences between simulation and measurement results may be caused in inaccurate models as well as the fact that we only consider the threshold voltage variations as the TID effects, neglecting other parameters including mobility variation.

V. CONCLUSION

We have designed, analyzed and measured TID effects of a 3GHz VCO with symmetric load implemented in a 0.25μm Silicon-on-Sapphire (SOS) CMOS process. Based on our simulation and pre- and post-radiation measurement results, we can draw the following conclusions: a) The TID effect will cause VCO tuning range and center frequency to change; b) the TID may make it more difficult for the VCO to start up oscillation; c) the TID may cause higher VCO jitter. For a symmetric load, the load working in linear region contributes less jitter than that in the saturation region.

VI. ACKNOWLEDEMENTS

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