Total Ionization Dose Effects and Single-Event Effects Studies of a 0.25 μm Silicon-On-Sapphire CMOS Technology

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I. INTRODUCTION

Silicon-on-Sapphire (SOS) CMOS is an attractive technology for radiation-tolerant circuits design. It eliminates single-event latch-up and has a smaller sensitive volume for single-event upsets (SEUs) and single-event transients (SETs) compared to Bulk CMOS technology [1, 2]. However, like any Silicon-On-Insulator technology, SOS technology has back-channel leakage as part of the total ionization dose (TID) effects [3, 4].

We are exploring the applicability of a commercial SOS technology for the front-end readout ASICs in the optical link systems for the ATLAS [5] upgrade at the Large Hadron Collider [6]. This paper presents detailed studies of both the TID and single-event effects (SEE) in Peregrine's 0.25 μm Silicon-On-Sapphire (UltraCMOS®) process. A test chip with various test structures was designed and fabricated using this technology. The chip was irradiated with a Co-60 gamma source for TID study and with a 220 MeV proton beam for SEE study, both up to a dose comparable to that in our application. Reported here are the TID and SEE results with a dose up to 100 krad.

Our results show that with a grounded sapphire substrate, the overall leakage current including back-channel leakage becomes negligible; the threshold voltage variations due to radiation for NMOS and PMOS are mitigated to about 55mV and 45mV respectively. The technology also demonstrates good SEE immunity.

II. THE SOS CMOS TEST CHIP

The basic features of the 0.25μm SOS CMOS technology used in the test chip are given in Table 1.

Table 1. The Technology features of the test chip

VDD	2.5V
Gate Oxide Thickness	6 nm
Process	0.25μm Silicon-on-Sapphire CMOS
Device isolation	LOCOS
Interconnectivity	3 metal layers
NMOS polysilicon gates doping	N+
PMOS polysilicon gates doping	P+

The test chip contains an 8×12 array of NMOS and PMOS transistors with different channel widths (80 and 40 μm) and lengths (0.25, 0.5, and 1.0 μm), implemented in four different types of layout: 4-finger, 8-finger, and 16-finger, all in standard layout, and enclosed-layout transistor (ELT) [7]. Since the edge leakage current is proportional to the number of edges in a transistor, the comparison between the leakage current in ELT and multi-finger transistors provides information on how much the back-channel leakage and edge leakage contributes to the total leakage current. To minimize the effects of process variations, each transistor of a particular size and layout has three identical copies. The transistors are spread out in the transistor array for better measurement statistics.

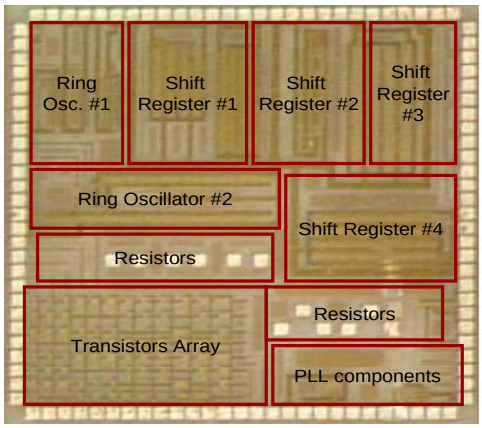

Figure 1: Photograph of the SOS test chip

III. MEASUREMENT RESULTS AND DISCUSSION

A. TID results

To characterize the TID effects, the I-V characteristic curve of each transistor is measured using a picoameter and three programmable DC power supplies. The current I_D is measured as a function of V_{GS} before and after the radiation while V_{DS} is fixed at 0.1V for NMOS and –0.1V for PMOS. The V_{GS} sweeps from 0 to 1.5V when measuring NMOS transistors and from -1.5 to 0 V in the PMOS case.

The test chips were irradiated with a Co-60 gamma source up to 100 krad(Si) followed by annealing studies at room temperature. Two different setups for the test chips were carried out during the irradiation: with the sapphire substrate left floating and with the substrate grounded.

1. With the sapphire substrate floating.

In the first TID test, the sapphire substrate of the chip was left floating. During irradiation the NMOS transistors are biased with V_{DS} = 2.5 V and the PMOS with V_{DS} = -2.5 V.

Shown in Fig. 2 are the I-V curves of NMOS and PMOS transistors (W/L = 40/0.25 um, ELT) before and immediately after the irradiation at two different total doses with a dose rate of 1.2 krad/hr. At a low dose (33 krad(Si)), the I-V curves of the NMOS transistors shift left (Vt decreases) as the leakage current increases. At a high dose, the I-V curves shift right (Vt increases) without an increase in leakage current. In contrast to the NMOS case, the I-V curves of PMOS transistors (W/L = 40/0.25um, ELT) stay unchanged at the low dose (≤ 33 krad (Si)) but move left (|Vt| decreases) at high dose (86 krad (Si)) with an increase in leakage current. This observation indicates that the net trapped charge in both PMOS and NMOS devices is positive at low dose and becomes negative at high dose. This result is new compared to what have been reported in literature. In [3, 4], trapped positive charge is believed to induce leakage current in NMOS, but not in PMOS. In [10] trapped negative charge is believed to induce the leakage in PMOS, but not in NMOS.

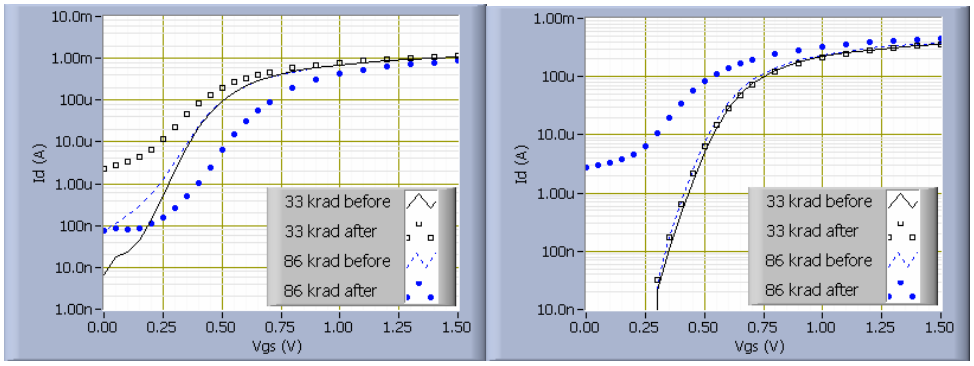

Fig. 2. The I-V curves of NMOS (left) and PMOS (right) ELT transistors

Shown in Fig. 3 is a study on the contribution of edge and back channel leakage to the total leakage current. The transistors of size (40µm, 0.25µm) were irradiated at 1.2krad/hr. From the figures we see that the leakage current in standard layout transistors is higher than that in an ELT for both PMOS and NMOS; and the back-channel leakage current accounts for a large portion of the overall leakage current (about 30% for a 16-finger transistor and about 50% for a 4-finger transistor).

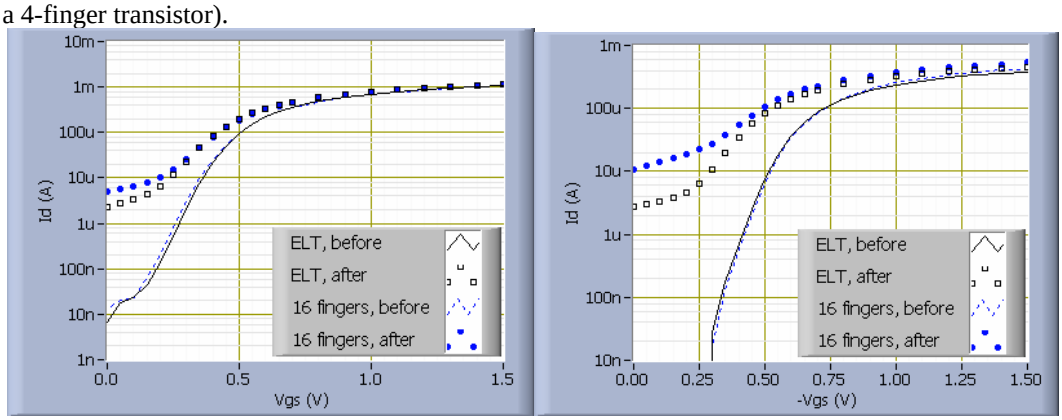

Fig. 3 The layout effect on NMOS (left) and PMOS (right) transistors

The leakage current vanishes in for both NMOS and PMOS after a 120-day of annealing at room temperature, indicating that the leakage current would not be a problem in realistic dose rate in our applications. The annealing has no significant effect on the threshold voltage shift. The annealing process is roughly linear with a logarithmic time axis, indicating that the dominating annealing process follows the tunneling annealing model [11].

2. With the substrate grounded.

We did a second on-line TID measurement on the test chip with the sapphire substrate grounded at 0V. During irradiation and the measurement, the NMOS transistors are biased with V_{DS} = 0.1 V and the PMOS with V_{DS} = -0.1 V.

With the substrate grounded, we observed that the leakage current in both NMOS and PMOS becomes negligible, both during and after the irradiation. This is shown in figure 4. In addition, the threshold voltage shift is also greatly reduced, with about 180 mV of increase in Vtn for NMOS (W/L = 40/0.25 um, 16 fingers) and 90 mV of decrease in |Vtp| for PMOS (W/L = 40/0.25 um, 16 fingers).

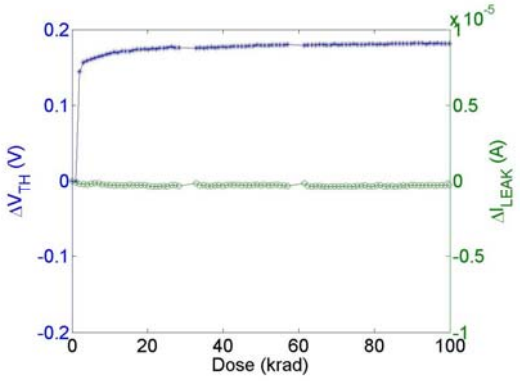

Figure 4 (a) NMOS threshold voltage change (left) and leakage current after 100Krad irradiation. NMOS W/L=40/0.25 16 fingers

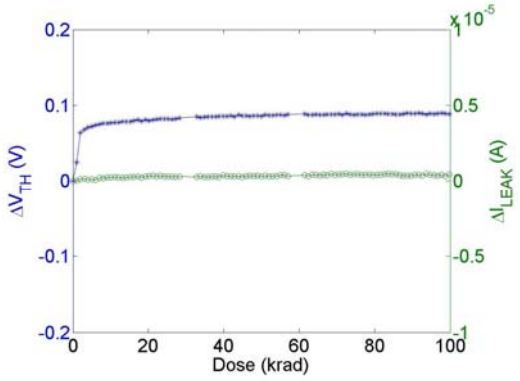

Figure 4 (b) PMOS threshold voltage change and leakage current after 100Krad irradiation. PMOS W/L=40/0.25 16 fingers

B. SEE results

An online test was done on the shifter registers in the chip at a dose of 100krad under a 220 MeV proton beam. A pseudo random bit stream was written into these test elements at a rate of 40Mb/s during irradiation. The outputs of the test elements were compared with their respective inputs for errors. No errors were reported before, during and after irradiation period. The current consumption of these test elements was monitored. Relating to the functionality of our test structures, there was no significant current change that inhibited device operation. When comparing standard geometry based shift registers to enclosed geometry based shift registers, there was no difference in functionality and SEE immunity. In addition, since the standard geometry based shift register worked error free for the given radiation period, the resistive hardening technique showed no further benefit in relation to SEE immunity. From the results of the test elements up to 100krad, we report that typical SEU's and SEB's were not seen in our experiment on the 0.25 μm (UltraCMOS®) technology. Table 2 shows fluence, error count # and cross section data for the different type of test elements in our experiment.

Table 2. Fluence, Error Count # and Cross Section Data for Test Elements

Test Element Type	Fluence(proton/cm^2)	Error Count #	Cross section(cm^2)
Std Shift Register	$1.8*10^{12}$	0	$<5.6*10^{-13}$
ELT Shift Register	$1.8*10^{12}$	0	$<5.6*10^{-13}$
Res. Hard Shift Register	$1.8*10^{12}$	0	$<5.6*10^{-13}$
SET free logic latch	$1.8*10^{12}$	0	$<5.6*10^{-13}$

IV. CONCLUSION

We have performed detailed studies of both TID and SEE effects in Peregrine's 0.25 μm Silicon-On-Sapphire (UltraCMOS®) process. Our test results show that with the sapphire substrate being grounded, the overall leakage current including back-channel leakage for both NMOS and PMOS are negligible during and after irradiation; the threshold voltage variations due to TID for both NMOS and PMOS are mitigated down to about 55mV and 45mV respectively. SEE test results show that this process has exhibited SEE immunity up to 100krad of radiation.

V. ACKNOWLEDEMENTS

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