An Optical Demo-Link for ATLAS Inner Detector Readout Upgrade

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Abstract

The GOL ASIC is a serializer chip developed by CERN based on a 0.25 μm CMOS technology [1]. The GOL operates with two data rates: 800 Mbps and 1.6 Gbps. This ASIC has been evaluated with radiation tolerance requirement for the ATLAS Inner Detector upgrade for the SLHC[1]. A demo-link has been designed and constructed to read out silicon detectors in the test staves through fiber optics. Through this demo-link we plan to study system issues in a giga-bit optical link. This concept will be extended to future serializer ASICs like the GBTx and the LOC when they become available. Experience gained from these demo-links will help us design and build a reliable optical readout system for new ATLAS Inner Detector readout.

I. Introduction

R&D activities for ATLAS Inner Detector upgrade, especially its B-layer replacement, have taken place for several years. On the detector side, a stave concept has taken shape. A stave is a mechanical structure on which the silicon sensors and front-end readout ASICs (called the hybrid module) are placed. The stave provides support to services like power supplies and cooling tubes. The stave also is a natural unit to gather data from the hybrid modules, process and serialize them and send the data off the detector to the back-end electronics through optical fibers.

Together with the development of new silicon sensors for the upgrade, new front-end readout ASICs are being developed with newer technologies to meet new requirements. With these developments, a new front-end readout system is in discussion. In this system an optical link with a data rate at multi-giga-bit per second is proposed to meet new demands. All developments for the front-end readout electronics need to meet the radiation tolerance requirements for the ATLAS Inner Detector at the SLHC. This includes the transmitting part of the optical links.

Giga-bit range serial data transmission has its own specific issues. Many of these issues were discovered and addressed in the present optical links like the one for ATLAS Liquid Argon calorimeter front-end readout. Lessons have been learned from those exercises and are documented [2]. In the new optical readout for the Inner Detector upgrade, we propose the demo-link concept to develop the optical link together with not only the ASICs (GBTx, LOC) and subsystems (the Versatile Link) for the optical link itself, but also the detector's other front-end readout ASICs. This way we can understand issues in the link, in integration, installation and system reliability at early stages so that actions can be taken to address them. With this, we hope to have a high quality, reliable optical link for the ATLAS Inner Detector upgrade.

There are two ASIC developments (GBTx and LOC) to meet the new data rate and radiation tolerance requirements for the upgrade. These ASICs are not yet available for system development. The presently available ASIC in giga-bit data rate range is the GOL chip which has been verified for applications in LHC. We verified it to the SLHC radiation tolerance requirements and started the first demo-link with this ASIC. We are prepared to move to the GBTx and LOC ASICs when they become available.

In this note, we report the irradiation test results on the GOL ASIC in section II. In section III the GOL based demo-link is described. The integration of this demo-link with stave-06 is reported. In section IV, we outline the design consideration for the GBTx and LOC based demo-link. It will be this demo-link that will lead to the baseline design of the optical link for the ATLAS Inner Detector readout upgrade. Conclusions and acknowledgements are in section V.

II. Irradiation tests on the GOL ASIC

The GOL ASIC has been qualified for applications in the LHC radiation environment [3]. We irradiated two of the GOL chips with a 230 MeV proton beam and find that this chip may be used in the SLHC radiation environment. Detailed test results have been reported elsewhere [4]. Here we summarize the characteristics of the GOL chip before and after the irradiation (total ionization dose effect) and the single event effect measurement results.

A. The total ionization dose effect

The eye diagrams of the serial output of the GOL before and after the irradiation are shown in Figure 1. There is no change in rise/fall times of the waveforms. The amplitude decreases from 350 mV to 300 mV. The eye opening easily pass 1.6Gbps eye mask test adopted from the Gigabit Ethernet standard.

[1] The work reported in this note is supported by the US-ATLAS for the high luminosity upgrade of the LHC.

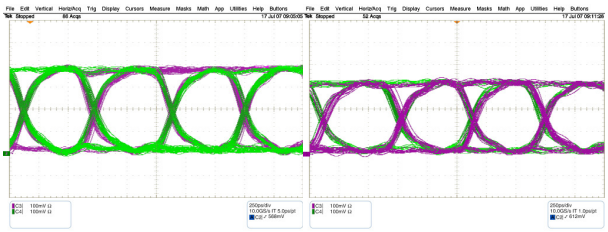

Figure 1: Eye diagram of the GOL serial output before (left) and after (right) the irradiation with 230 MeV protons.

Jitter measurements were performed before and after the irradiation and are summarised in Table 1. The radiation effect on the jitter components is minimal.

Table 1: Measurement on the GOL jitter components before and after the irradiation

jitter component	clock (ps)	before (ps)	after (ps)
random (RMS)	8.6	8.8	9.9
Deterministic (pk-pk)	10.8	112.5	96.6
total at BER < 1E-12	127.7	208.6	205.2

Jitter transfer function of the GOL chip is shown in Figure 2. After the irradiation, low frequency jitter is more suppressed, while jitter frequency at around 1 MHz is slightly enhanced.

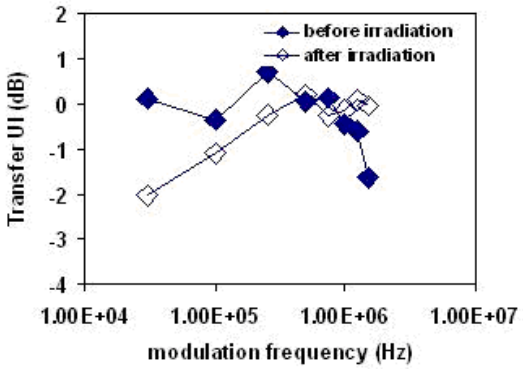

Figure 2: GOL jitter transfer function before and after the irradiation.

Jitter tolerance of the complete data link with TLK2500 as the deserializer chip was also tested. We measure the jitter penalty of equivalence to 1dB power degradation while maintaining better than 1E-12 bit error rate (BER). As shown in Figure 3, the applied sinusoidal jitter magnitude and frequency that caused the specified degradation follows SONET/SDH OC48 template well. Irradiation caused no effect on the overall timing margin.

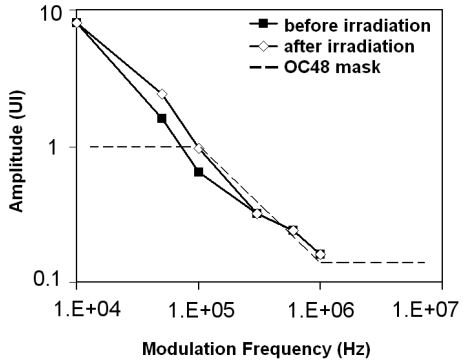

Figure 3: GOL-TLK data link jitter tolerance before and after the irradiation.

B. *Single event effect*

Two types of single event effects were measured during the irradiation with 230 MeV protons: data bit corruption that does not bring down the link synchronization and the event that cause the link to lose synchronization hence a re-synch was needed to establish the serial data transmission.

Table 2: Single event effect measurement a GOL-TLK link system with the GOL under proton irradiation.

SEE type	Cross section (cm^2)
loss of synch	$< (2.5\pm0.6)\times10^{-13}$
bit corruption	$< (5.3\pm2.6)\times10^{-14}$

In conclusion, the GOL ASIC is suitable for optical link system development for applications in the SLHC.

III. THE GOL BASED DEMO-LINK

Since the GOL is the only serializer chip that has been evaluated and verified to be radiation tolerant for applications in SLHC, we decided to start our demo-link with this ASIC. In this section we report on this demo-link and its integration with the stave-06 at the LBNL.

A. *The demo-link design and test*

Shown in Figure 4 is the block diagram of the GOL based demo-link. We employ a four board system so that the two interface boards are simple and can be easily re-designed and constructed to meet the requirements of different stave configurations. As a matter of matter, we are designing new interface boards to read out the stave-07.

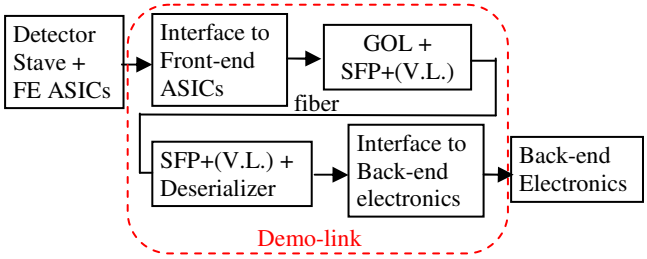

Figure 4: GOL-TLK demo-link block diagram. Shown in the dashed line box is the demo-link, which takes data from the stave and transmit it to the back-end electronics via optical fiber.

The choice of the TLK2500 as the deserializer is based on past experience with this commercially available chip, and for economical reasons. TLK2500 is a serializer-deserializer (ser-des) chip produced by Texas Instrument. This ser-des has a data rate up to 2.5 Gbps, matches perfectly with the GOL. Embedded ser-des in FPGAs are much more expensive than TLK2500 and are reserved for the GBTx and LOC based demo-links that operate at higher speeds. Shown in Figure 5 is a picture of the GOL based demo-link. The optical interface is chosen to be SFP+ format. This is the standard chosen by the Versatile Link project. Please see reports on the Versatile Link in the joint ATLAS-CMS opto-electronics working group session in this conference. Shown in Figure 6 is the optical eye diagram.

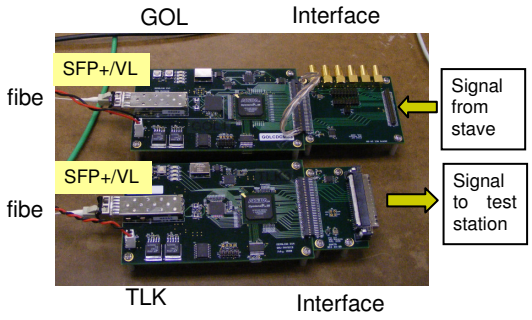

Figure 5: Picture of the GOL-TLK demo-link.

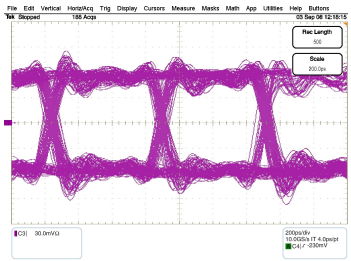

Figure 6: Optical eye diagram of measured from the GOL-TLK demo-link.

Bit error rate of this demo-link was measured in lab to be better than 1E-14 before we carried out the integration test with the stave-6.

B. The integration with the stave-06

The stave -06 is a prototype stave with 6 hybrid modules. The present ATLAS Inner Detector front-end readout ASICs are used to readout the silicon sensors. The GOL based demo-link was successfully integrated between the stave-06 and its readout test stand (functions as the back-end electronics). Although digital data was transmitted correctly, we discovered noise issues due to the introduction of this high speed serial data link. This issue has been investigated and will be corrected in the new interface board for the stave-07. This illustrates the importance of the demo-link. More system tests are in line with this demo-link until the faster GBTx and LOC based demo-links are available.

IV. Design Considerations for GBTx and LOC Based Demo-Link

New front-end electronics systems for the SLHC must withstand higher radiations. The data transmission must meet with higher data rate requirements. New radiation tolerant ASICs are being development to meet the new demands. There are two ASIC developments for optical links: the GBT and the LOC. Please see reports on the GBT in TWEPP 2007, LOT in this conference. The ser-des part of the GBT is called the GBTx. The LOC is only a serializer chip. Both ASICs couple to the Versatile Link, and operates at a serial data rate around 5 Gbps. The block diagram of the GBTx and LOC based demo-link is shown in Figure 7. In this design, we make use of the Reference Link project [?] which is currently under development as a common project between ATLAS and CMS for the SLHC upgrade. The Reference Link is FPGA based, with the ser-des function realized with the embedded ser-des in the FPGAs. By the time when the GBTx and the LOC are available, we anticipate that prices for the ser-des embedded FPGAs would fall into reach in one year's time.

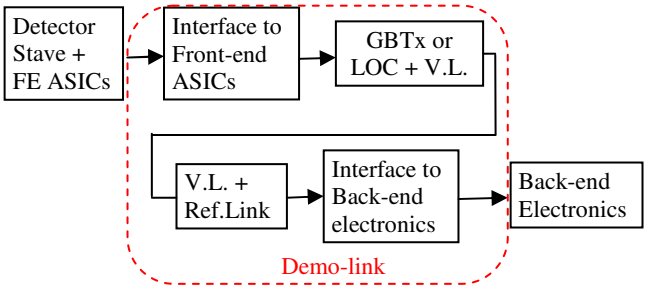

Figure 7: The GBTx or LOC demo-link block diagram. In this design, common projects such as the Versatile Link and the Reference Link are incorporated to minimize the R&D efforts.

V. Conclusions and Aknowledements

The GOL based demo-link has been constructed and system level studies are being carried out with silicon detector and its front-end readout ASICs (the stave). The next generation of the demo-links will be based on the GBTx and the LOC, both currently under development. In this new demo-links, developments from common projects such as the Versatile Link and the Reference Link will be incorporated to minimized R&D efforts.

We would like to thank the US-ATLAS program which provides funds for this R&D effort. We also would like to thank many of our colleges who have been helping us in defining, designing, construction and testing of this demo-link. Particularly we would like to thank Vataliy Fadeyev and Jason Nelson from SCIPP, Carl Habor from LBNL, P.K.Teng and Suen Hou from IPAS in helping us in the demo-link efforts. We would like to thank Jim Kierstead at BNL and Ethan Cascio at MGH's NPTC for their help in irradiation tests.

VI. References

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