Status Report on the LOC ASIC

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Abstract

Based on a commercially available 0.25 μm Silicon on Sapphire CMOS technology, we are developing the LOC ASIC for high speed serial data transmission in the front-end electronics systems of the ATLAS upgrade for the SLHC[1]. Evaluation of this technology for applications in the SLHC, based on a dedicated test chip, has been performed with irradiation tests in gamma (Co-60) and in 230 MeV proton beams. Test results indicate that this may be a candidate technology of ASIC developments for the SLHC. More thorough evaluation tests will be carried out under another R&D program supported through the Advanced Detector Research (ADR) from the Department of Energy. Characterization tests on the first prototype serializer, LOC1, have been carried out in lab. Based on the lessons learned from this chip, we propose a new architecture design of the second prototype, LOC2, aiming for a serial data rate in the range of 5 Gbps. Simulation on key components of LOC2 are being carried out and the results we have so far are presented in this note. LOC2 is scheduled to be submitted for fabrication in the first half of 2009.

I. INTRODUCTION

Detector and its readout system upgrades for the high luminosity upgrade of the LHC (SLHC) call for higher bandwidth optical links that withstand higher radiation levels. R&D activities for ATLAS Liquid Argon Calorimeter readout upgrade have taken place for several years. In this R&D program, we propose the LOC (link-on-chip) ASIC as a serializer based on a commercially available 0.25 μm Silicon on Sapphire (SOS) CMOS technology. The initial idea was to integrate "everything" into one chip, including the optical interface. Fiber would be coupled directly to the chip to spare high speed copper traces on the PCB. This project started out with the SOS technology evaluation. This work produced encouraging results which indicate that this technology may be a candidate of ASIC developments for the SLHC. More thorough evaluation tests grow out of the scope of the present R&D work for the ATLAS upgrade, and hence are to be carried out under another R&D program supported through the Advanced Detector Research (ADR) from the Department of Energy. The first prototype serializer, LOC1,

was designed with collaborative effort between the electrical engineering and the physics departments at SMU. This first prototype provided valuable information on key components, especially the PLL and the serializer structure, for the LOC2 design. The second prototype, LOC2, is the one to be reported in detail in this note.

We begin our report on the SOS technology evaluation in radiation environment, in section II. In section III we briefly report the test results on LOC1. In section IV, we outline the design considerations for LOC2, based on lessons learned from LOC1. We also present the simulation results we have so far on key components of the LOC design. These simulation results indicate that a 5 Gbps serial data rate is hopeful. Conclusions and acknowledgements are in section V.

II. EVALUATION OF THE SOS TECHNOLOGY IN RADIATION ENVIRONMENT

The Silicon on Sapphire technology has been a choice for radiation tolerant electronics since the 1970s. With the insolating sapphire substrate, this technology eliminates the parasitic transistor in the bulk silicon substrate and hence removes the mechanism for circuit latch-ups. This insolating substrate also reduces the possibility of single event upset (SEU) because charged ions cannot travel as far in the components as in bulk silicon substrate [1, 2]. The only limiting factor of this technology in the past was that it was difficult to achieve high yields in volume production thus this technology was limited to very specialized applications in military and space programs. In the early 1990s, semiconductor manufacturers solved the problem of crystallization defects in silicon grown on sapphire [3] and brought this technology to market through the same equipment for the bulk silicon CMOS process. Thanks to the fast expansion in the wireless and broadband markets, the SOS technology, which finds a lot of applications in RF and mixed signal circuits there, is on a fast-growing path.

In order to evaluate this technology for ASIC developments for the SLHC, we designed a dedicated test chip in collaboration with the electrical engineering department at SMU, and conducted irradiation tests on the total ionization dose (TID) effect and the single event effect (SEE). A picture of this test chip is shown in Figure 1. The TID effect was measured through transistor I-V curves with the transistor array in the test chip. The SEE was measured with dynamic data transfer through the shift registers in the test chip under irradiation. Detailed report on this work has been published elsewhere [4]. We only summarize the key results here.
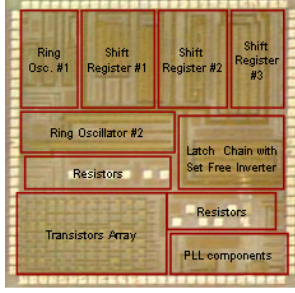

Figure 1: Image of the SOS test chip with marks for the test units imposed on the image.

A. The total ionization dose effect

The TID tests were carried out with gamma irradiation (Co-60). The chip substrate was grounded during irradiation. Transistor I-V curves were measured repeatedly while the test chip was under irradiation. Radiation induced leakage current and threshold voltage changes were plotted as a function of total accumulated dose. The results are shown in Figure 2.
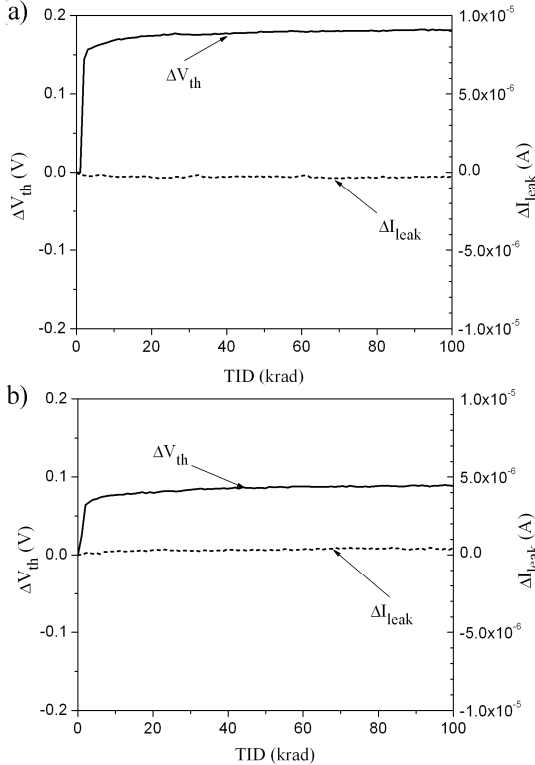

Figure 2: Irradiation induced leakage current and threshold voltage change as a function of total ionizing dose. Plotted in a) are for the NMOS transistors, b) for the PMOS.

There is almost no leakage current change measured. The small threshold voltage change happened at the very beginning of the irradiation and then remains almost unchanged with the increase of the total dose. This change is within the technology variation and is considered acceptable in ASIC designs.

B. Single event effect

Single event effect was measured through online monitoring of the data bits shifted through registers and logic latches in the test chip under irradiation of a 230 MeV proton beam with a flux of 7.7×10^8 proton/cm^2/s. No error was observed before, during and after the irradiation periods. The zero error result is translated into a cross section upper limit of 5.6×10^{-13} cm^2 for all four tested units (standard layout shift registers, enclosed layout shift registers, resistively hardened shift registers, and latches).

We concluded from these tests that this technology may be a good candidate for ASIC development for SLHC and we decided to use it in our LOC development.

III. LOC1 TEST RESULTS

The first prototype serializer, LOC1, was designed in collaboration with the electrical engineering department at SMU. In this prototype, we planned to check four key components: the serializing unit, the PLL and clock unit, the electrical output CML driver and the VCSEL driver. Shown in Figure 3 is the block diagram of LOC1. A self-biasing PLL was chosen for the high speed clock generation. This choice was made based on this PLL's good noise rejection and wide tuning range. Self-biasing PLL also has the reputation of independent of manufacturing process [5]. We measure a tuning range of the PLL in LOC1 from 0.8 to 2.4 GHz with a random jitter of about 4 ps at 1.25 GHz. Choice of static D-flip-flop for SEE immunity consideration led to a four-arm 5:1 shift serializer with two stage 2:1 multiplexer structure for the serializing unit. This design turned out to be a major source of the deterministic jitter (DJ) in the output serial bit stream. The CML driver did not work to the design specification but good enough for us to conduct measurements of this chip. We did not succeed in the VCSEL driver design.
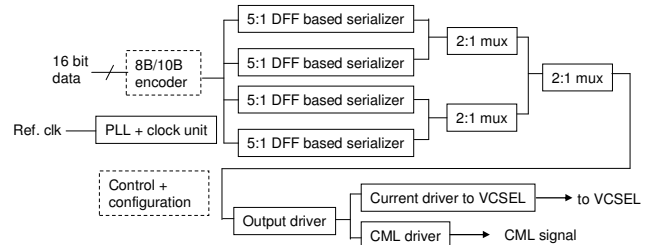

Figure 3: Block diagram of LOC1. Solid line boxes are implemented in the ASIC, dashed line boxes are implemented in FPGA for testing purpuses.

An eye diagram with a 2^7-1 pseudo random input is shown in Figure 4. The data rate is 2.5 Gbps. Large DJ is observed and traced back to the serializing unit. This problem will be corrected in future designs.
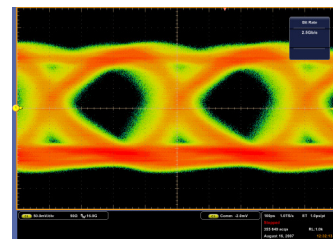

Figure 4: Eye diagram from LOC1 output with 2^7-1 pseudo random input.

A bit error rate bathtub curve at 2.5 Gbps is also measured. The best BER reached ~10^{-11}, indicating the digital logic in LOC1 is correct.
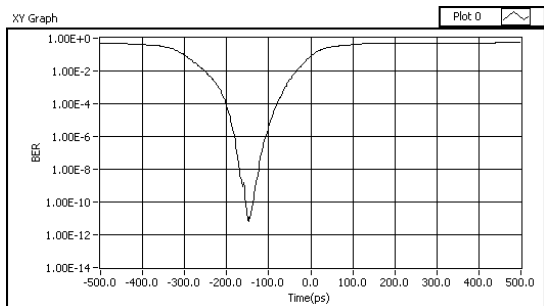

Figure 5: The bathtub curve in the bit error rate measurement of LOC1. Due to the large DJ, the best BER only reaches ~10^{-11}.

Valuable lessons are learned in the LOC1 design and testing. This helps in our LOC2 design.

IV. DESIGN CONSIDERATIONS IN LOC2 AND SIMULATION RESULTS

In the process of the LOC development, several common projects at CERN have started to develop ASICs and subsystems for the SLHC upgrade. Among them the most relevant project, of which we are a collaborator, is the Versatile Link project. Please see reports on the Versatile Link in the joint ATLAS-CMS opto-electronics working group session in this conference. We decide to move the optical interface of the LOC ASIC into the Versatile Link and concentrate on the serializer design. On the input of LOC, we also realize that it is impossible to have one input interface that meets with demands from the upstream electronic systems from both ATLAS Inner Detector and Liquid Argon Calorimeter. With this we now re-define the LOC as a 16:1 serializer chip or function block, with CML output to be connected to the transmitter part of the Versatile Link. We move the user interface function, together with the framing/encoding function into another chip or function block. For the second prototype, LOC2, this is the combination of the two function blocks with some configure and control unit. This is shown as block diagram in Figure 6.
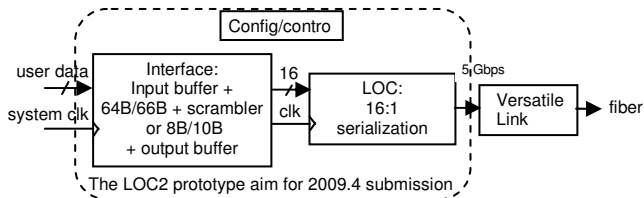

Figure 6: LOC2 block diagram (in dashed line box). The output of LOC2 connects to the Versatile Link

The interface chip or function block takes the data and its clock from the "user" or upstream electronics, and prepare for the data and clock for the 16:1 serializer which is the core part of the LOC. With this design, the core part of the LOC development is somewhat decoupled from individual user requirements. This helps the LOC development at the stage when the user interface cannot be finalized. Shown in Figure 7 is the block diagram of the interface unit.
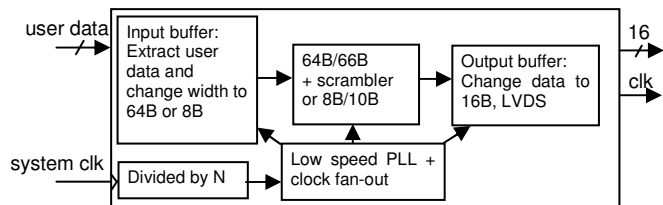

Figure 7: The interface unit block diagram.

The core part of the LOC ASIC, the 16:1 serializer can now be implemented as shown in Figure 8. The logic structure is then much simpler than a 20:1 serializer. The fundamental structure in the serializing unit is two D-flip-flops and a 2:1 MUX. In this cascade structure, only the last stage of the 2:1 multiplexing runs at 2.5 GHz for a 5 Gbps serial data output. Effort can then be concentrated on this stage to maximize the speed. The clock fan-out unit is also simplified to a "divide-by-2" chain. The key components in this design are the 2.5 GHz PLL, the static D-flip-flop and the final CML driver that works at 5 Gbps. In the following we will present the simulation results we have on some of the key components.
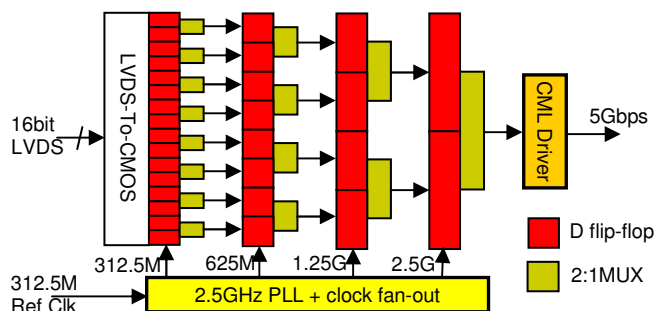

Figure 8: The interface unit block diagram.

First of all, we used a simple inverter to adjust the PMOS/NMOS transistor ratio to equalize the delay from logic 1 to 0 and from 0 to 1. This ratio is found to be n×(1.9/1.4), where n = 1,2,3,…. Both basic and multi-finger layouts are checked to maximize the speed. The delay of an inverter, when driving itself, is found to be 32 to 35 ps, corresponding to a frequency of about 30 GHz. This is comparable with speeds achieved in 0.13 to 0.15μm bulk silicon CMOS technology. For a comparison, we made a simulation of the same inverter in a 0.25μm bulk silicon CMOS technology and found that the delay time is 60 ps under the same condition, about a factor of 2 slower than the SOS CMOS technology.

Simulation on the D-flip-flop (DFF) started out with the C^2MOS type as used in the GOL ASIC [6], but we soon moved to the TGDFF which is about 20% faster than the C^2MOS DFF, and has at least the same SEE immunity [7]. Different transistor size, single and multi-finger layouts have been checked to minimize the delay or maximize the speed. The minimum decay is found to be 292 ps in the slowest (the SS corner) case. This indicates a 5 Gbps serializer possible because the time needed for the basic unit (DFF+MUX) is 400 ps.

The design work on the PLL and the CML driver is in progress and will have to be reported at a later time. In

conclusion, the architecture of the LOC2 differs a lot from the LOC1. The design work for the LOC2 is on track and so far a 5 Gbps data transmission seems achievable.

V. CONCLUSIONS AND AKNOWLEDEMENTS

The LOC ASIC design evolves with time. We incorporate into our LOC design the development from the Versatile Link project and decide to move the optical interface from the LOC to the Versatile Link. The LOC now is proposed to be a 16:1 serializer as its core part. Different interface ASICs or function blocks will be developed according to the application of the LOC.

Technology evaluation on the 0.25μm SOS technology produced encouraging results and enables us to go ahead with the LOC design using this technology. More studies will be performed on this technology with support from the ADR program.

The design work for the present prototype, LOC2, is in progress. Simulations on critical components indicate that a 5 Gbps serial data rate is hopeful.

VI. REFERENCES

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