Electronics of the Atlas Liquid Argon Calorimeter and its Precision Calibration

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On behalf of the ATLAS Liquid Argon Calorimeter Group

***Abstract*–The Liquid Argon sampling calorimeter is a key detector component in the ATLAS experiment at the LHC, designed to provide precision measurements of electrons, photons, jets and missing transverse energy. In this note we present the detector readout electronics system and its precision calibration. The system has 182,468 channels with more than 16-bit dynamic range. The contribution to the relative energy resolution constant term due to the calibration uncertainty is below 0.25%. The radiation tolerant optical link between the detector front-end and the data acquisition back-end is also discussed.**

I. Introduction

ATLAS is a general-purpose particle physics detector designed for operation at the Large Hadron Collider (LHC) at CERN. The LHC is a proton-proton collider with a design center-of-mass energy at 14 TeV. The ATLAS detector comprises an inner tracking system, a calorimeter system and a muon spectrometer. In the calorimeter system the liquid argon (LAr) calorimeters make up the electromagnetic barrel calorimeter and the electromagnetic and hadronic endcap calorimeters, covering a pseudo-rapidity region up to $|\eta| = 4.9$.

The electronic readout of the LAr calorimeters is divided into a Front-End (FE) system of boards mounted in custom crates (the front-end crates or FEC) directly on the cryostat feedthroughs inside the ATLAS detector, and a Back-End (BE) system of VME-based boards located in an off-detector underground counting house. The requirement from physics to measure energy deposition from 30 MeV to 3 TeV in one calorimeter readout cell dictates the readout dynamic range. The energy resolution of the order of $10\%/\sqrt{E}$ (GeV) with an overall constant term not larger than 0.7% puts requirement on the electronic calibration contribution to the latter to be below 0.25%. [1] Detailed descriptions of the FE and BE electronics systems have been published elsewhere [2, 3]. In this note and in section II we describe the electronics readout system with emphasis on the optical link that connects the FE and BE electronics. In section III we outline the calibration procedure and present the results from the commissioning phase of the ATLAS detector. We conclude in section IV with acknowledgments to our collaborators in the ATLAS LAr Group who worked so hard in the past many years to design, construct and commission this detector.

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II. The ATLAS LAr Readout System

This LAr readout system is illustrated in Fig. 1. The FE electronics of the LAr comprises the front-end boards (FEB) which perform the readout and digitization of the calorimeter signals; the Calibration board which injects precision calibration signals to the readout system; boards for producing analog sums for the Level 1 trigger (TBB); and other control and monitoring boards. The FEC has its custom designed and built radiation tolerant DC power supply. The FEC is in a radiation environment with very limited access for maintenance [4]. The BE electronics has the Readout-Driver (ROD) boards as its core with many other service boards. The ROD performs digital filtering of the signals using an FPGA and DSP system. The BE electronics is accessible for maintenance during operation. A radiation tolerant optical link system operates at 1.6 Gb/s each fiber, and connects the BE to the FE electronics with 1524 channels.

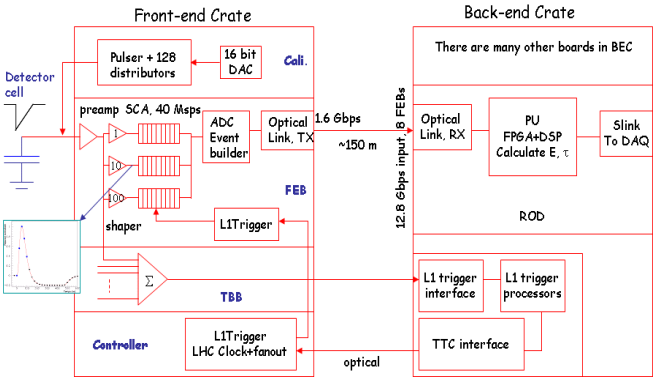

Fig. 1. The LAr readout system block diagram. The FEB and the ROD are the two main boards in this system for data acquisition and processing. The optical link operates at 1.6 Gb/s over about 150 m fiber and has its transmitting side on the FEB and must withstand the same level of radiation.

A block diagram of the FEB is shown in Fig. 2. A summary of the main specifications of the FEB is listed in Table I. After being amplified and shaped, the LAr calorimeter signals are sampled at the LHC bunch crossing frequency of 40 MHz and stored the SCA (sampling capacitor array). Once triggered, 5 samples around the peak are sent to the Analog-to-Digital-Converter (ADC). Digitized signals are built into the FEB event with header and control words and are sent off the detector through the optical link. There are 13 types of radiation tolerant Application-Specific-Integrated-Circuits (ASICs) used on the FEB. These ASICs have been developed

using technologies like the DMILL [5], the Deep-Sub-Micron (DSM) CMOS and the AMS BiCMOS. A limited number of commercially available components are used on the FEB (for example, the ADC and the serializer for the optical link). These components were evaluated to be radiation tolerant on production batch level.

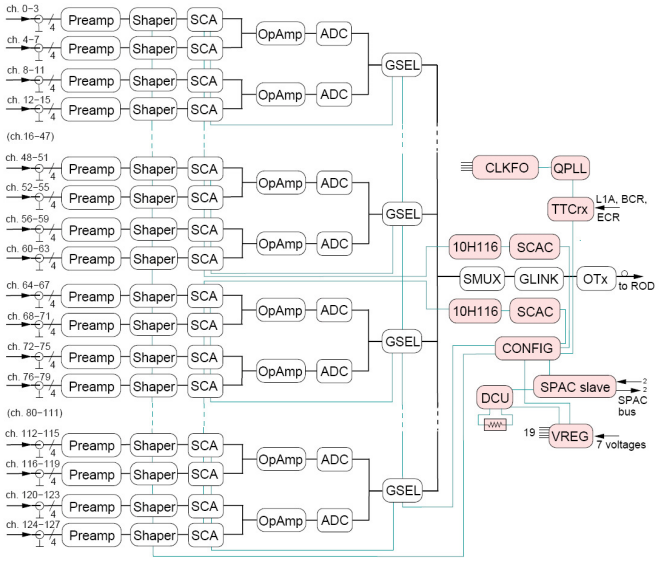

Fig. 2. The FEB block diagram showing all 128 channels. The Shaper has three gains (1×, 10× and 100×). Together with the 12-bit ADC, a dynamic range of about 17 bits is achieved.

TABLE I. SOME OF THE MAIN SPECIFICATIONS OF THE FEB

Channel count		Signal sampling	
Total Channels	182,468	Sampling frequency	40 MHz
Number of FEB	1,524	L1 trigger latency	< 2.5 μs
Channel density	128ch/FEB	Max. L1 trigger rate	75 kHz
Power consumption	≈ 0.7 W/ch.	Samples/channel	5 (typical) 32 (max)
		Deadtime	< Few %

Energy measurement		Time measurement	
Dynamic range	≈ 17 bits	Resolution	< 100 ps
Calibration uncertainty	< 0.25%		
Noise/channel	≈ 10 – 15 MeV		
Coherent noise/channel	< 5% of total noise/channel		

The block diagram for the optical link is shown in Fig. 3. FEB data after the ADC are organized into 32 bits at 40 MHz in LVDS format. The SMUX chip (an ASIC developed with the DMILL technology) [6] receives the parallel data and performs a 2:1 multiplexing to generate an output of 16 bits at 80 MHz. In addition, the SMUX generates a FLAG, which is HI (LO) for the MUX cycle when data from channels 0 - 63 (64 - 127) are sent the serializer (HDMP-1022 from Agilent Technologies [7] GLink chip set). The SMUX also performs a level shifting so that the data format match the input requirement of the GLink. The GLink adds protocol and control bits and produces a single serial output stream of 1.6 Gbps in PECL format. In the final step, this serial data stream is converted to an optical signal and transmitted off of the FEB via a custom-built optical transmitter (OTx) module which includes a commercial driver chip (SY88922V from Micrel Inc. [8]) and a 850 nm VCSEL (TTR-1A43 from TrueLight Corp. [9]) for converting the signal from electrical to optical. The choice of a VCSEL for the optical interface follows the trend in industry for short range optical networks. It is also based on the radiation tolerance that VCSELs demonstrate. Table II lists the parameters measured, and acceptance windows applied, during quality control (QC) measurements of the OTx. In addition, an eye mask test, and bit error rate tests at 0 dB and 10 dB attenuated optical power were also carried out. The bit error rates in both cases were required to be lower than 10^{-12}. Fig. 4 gives a typical eye diagram of the optical signal from the OTx. Detailed information about the QC tests of the OTx can be found in Reference [10].

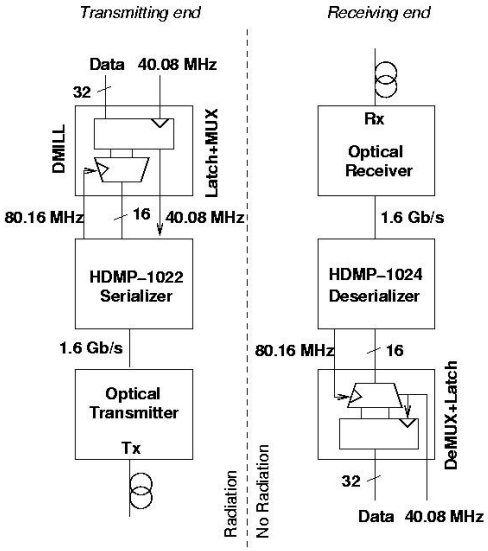

Fig. 3. The architecture of the transmission end (left side) and reception end (right) of the 1.6 Gbps FEB output data optical link. The transmitter is mounted on the FEB and the receiver on the ROD.

TABLE II. PARAMETERS MEASURED AND THE CORRESPONDING ACCEPTANCE WINDOWS DURING THE TESTS OF THE OTX MODULES

Parameters	Units	Min. Value	Max. Value
Average optical power	dBm	-7.5	-3.5
Extinction ratio	-	6.0	-
Rise time	ps	-	220
Fall time	ps	-	220
Deterministic jitter	ps	-	125
Random jitter (RMS)	ps	-	10

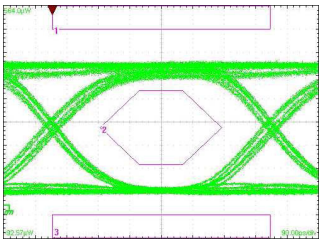

Fig. 4. An eye diagram demonstrating the eye mask test of a typical OTx module. The horizontal scale corresponds to 90 ps/division.

Multimode 50 μm core graded-index (GRIN) fiber is used to carry the signal from the FEB to the ROD. At the ROD end of the fiber, the 1.6 Gbps optical signal is converted back to an electrical signal via a PIN-diode based custom-built optical receiver (ORx) module. It is then de-serialized by the GLINK receiver (HDMP-1024) [7] back into an image of the 16 bits at 80MHz data stream output from the SMUX.

On the ROD data from the optical link is first processed in an FPGA to check data integrity. Data is also reformatted for the DSP to calculate for energy and timing information for each readout channel. The ROD data distribution block diagram is shown in Fig. 5. The processing unit (PU) employs DSPs to perform Optimal Filtering (OF) on the 5 data samples to calculate the peak amplitude (in ADC counts) and position (in time):

$$A_{max} = \sum_{j=1}^{N_{samples}} a_j(s_j - p), \quad (1)$$

$$\tau = \frac{\sum_{j=1}^{N_{samples}} b_j(s_j - p)}{A_{max}}. \quad (2)$$

where a_j and b_j are the OF Coefficients (OFC) computed from the normalized ionization pulse prediction [11] and the noise time autocorrelation [12]. Here p is the ADC pedestal.

Processed data is reformatted in another FPGA and monitored in some histograms. The data is sent off the ROD to down stream data acquisition system for further analysis. Shown in Fig. 6 is the signal on FEB after preamplifier and shaper with the detector pulse shape overlapped on it.

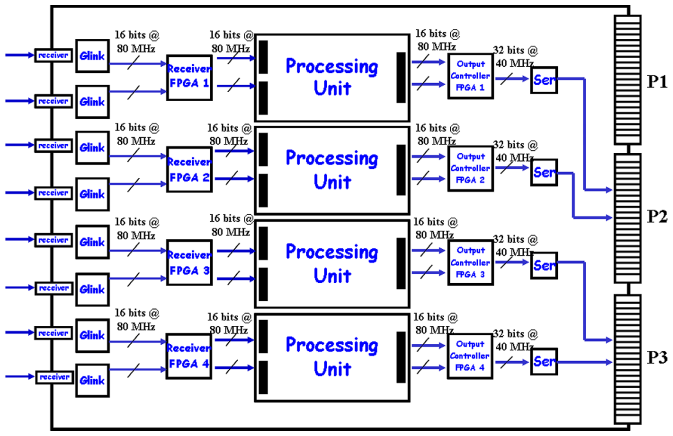

Fig. 5. Data distribution on the ROD board.

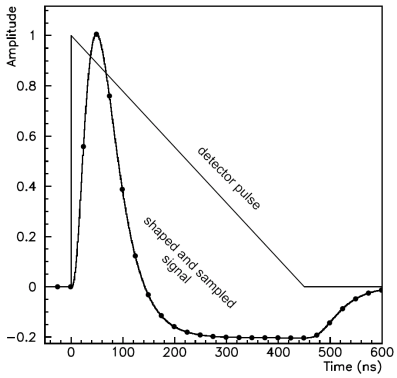

Fig. 6. Triangular pulse of the current in the LArg cell and the FEB output signal after bi-polar shaping. Also indicated are the sampling points every 25 ns. Even though a maximum of 32 samples can be attained, only a few samples (5 to 7) around the peak are typically used during normal data taking.

III. The Calibration of the LAr Electronics Readout

In order to translate the ADC counts into energy deposit in the detector cell, and to monitor the electronics readout system, its linearity and stability over time, a calibration pulse is generated by the Calibration board in the FEC with its amplitude set by a 16-bit DAC. This calibration pulse has a similar shape as pulses generated in the detector by passing ionizing particles. The following formula explains the needed steps to go from the amplitude A_{max} to the cell energy:

$$E_{cell} = F_{\mu A \to MeV} \cdot F_{DAC \to \mu A} \cdot \frac{1}{\frac{M_{phys}}{M_{cali}}} \cdot R \cdot A_{max} \quad (3)$$

$F_{\mu A \to MeV}$ depends on the sampling fraction and is estimated with GEANT4 simulations and results from testbeams. $F_{DAC \to \mu A}$ takes into account calibration board specificities. The R factor of Eq. (3) transforms ADC into DAC values. As R is determined on calibration pulse and not directly on ionization pulse, the difference between those two pulses has to be taken into account. The calibration signal is a decreasing exponential injected at the output of the detector cell, while the ionization pulse originates from a triangular signal collected by the electrodes. As a result, the shaper outputs of the ionization and calibration signal corresponding to the same initial injected current are different. The energy is corrected for the ratio of the two pulse maxima $1/(M_{phys}/M_{cali})$ in Eq. (3), the ionization pulse being predicted by factorization of the readout response [11]. All the constants of Eqs. (1), (2) and (3), except the $F_{\mu A \to MeV}$ factor, are determined by calibration runs, on a cell by cell and readout gain basis.

Frequent sets of calibration data are taken in order to test the stability of the different constants. An automated process has been put in place to reconstruct the data and prepare new sets of constants ready to be loaded in the ATLAS databases. The validation of those data is done with respect to a reference run. Databases are updated only if it is needed. From recent measurements, it has been observed that in stable operating conditions (mostly temperature) the parameter variations are small. Shown in Fig. 7 is the pedestal variation which is of the

order of a few MeV and well below the noise level. The relative maximum amplitude difference of the calibration pulses taken in a typical routine run, with respect to the validation reference, is shown in Fig. 8 is at the level of a few parts per thousand. In such a case a databases update is not foreseen.

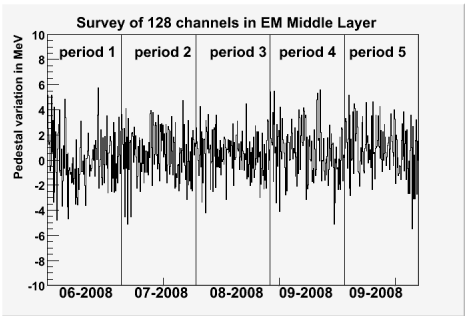

Fig. 7. Pedestal variation in MeV for different time periods, for a random set (1 FEB) of channels in the EM calorimeter.

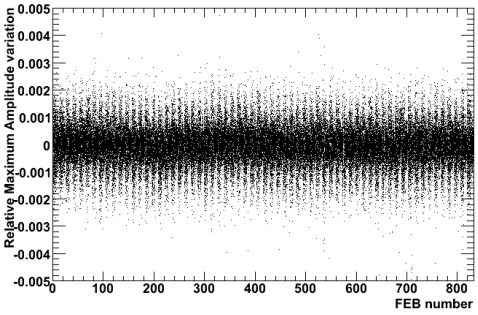

Fig. 8. Relative maximum amplitude variation of the calibration pulses in the barrel EM calorimeter.

IV. CONCLUTIONS

The ATLAS LAr readout electronics system is complex with its FE part operates in radiation environment with very limited access for maintenance. The BE process data based on an FPGA+DSP processing unit to obtain energy and timing information "on the fly". The radiation tolerant optical link system has 1524 fiber channels. Each fiber transmits data at 1.6 Gbps. This system is built based on commercially available parts and ASICs. The recent operation experience with the optical transmitter points to a reliability issue in the VCSEL that is under study. The LAr readout system is a key element in the LAr calorimeters to achieve an energy measurement with required precision dictated by physics goals. The OF for energy and time information calculation, and the calibration system are presented. The LAr calorimeter system with its readout electronics have been commissioned and are ready to take physics data.

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REFERENCES

[1] M. Aharrouche *et al.,* "Response uniformity of the ATLAS liquid argon electromagnetic calorimeter", *NIM A*582 (2007) 429.

[2] N.J. Buchanan *at al.,* "Design and implementation of the Front End Board for the readout of the ATLAS liquid argon calorimeters", *JINST* 3 (2008) P03004.

[3] A. Bazan *at al.,* "ATLAS liquid argon calorimeter back end electronics", *JINST* 2 (2007) P06002.

[4] N. J. Buchanan *at al.,* "Radiation qualification of the front-end electronics for the readout of the ATLAS liquid argon calorimeters", *JINST* 3 (2008) P10005.

[5] M. Dentan *et al.,* "DMILL, A Mixed Analog-Digital Radiation-Hard BiCMOS Technology for High Energy Physics Electronics", *IEEE Trans. Nucl. Sci.* 43 (1996) 1763.

[6] D. Dzahini, "Development of a DMILL Radhard Multiplexer for the ATLAS GLink Optical Link and Radiation Test with a Custom Bit Error Tester" Seventh Workshop on Electronics for LHC Experiments (2001) Stockholm, available at http://cdsweb.cern.ch/record/588659.

[7] Detailed information about the GLINK chipset and protocol is posted at http://literature.agilent.com/litweb/pdf/5966-1183E.pdf.

[8] Data sheet for the Micrel SY88922 laser diode driver, available at http://www.micrel.com/_PDF/HBW/sy88922v.pdf

[9] Information about the TrueLight TTR-1A43 VCSEL TOSA is available at http://www.truelight.com.tw/detail/41052/41052.html.

[10] T. Liu et al., "Quality Control Test of Optical Transmitters in Liquid Argon Calorimeter Readout System", ATL-LARG-PUB-2005-004, available at https://edms.cern.ch/document/882033/1.

[11] D. Banfi, M. Delmastro and M. Fanti, "Cell response equalization of the ATLAS electromagnetic calorimeter without the direct knowledge of the ionization signals", *JINST* 1 (2006) P08001

[12] W.E. Cleland and E.G. Stern, "Signal processing considerations for liquid ionization calorimeter in a high rate environment", *NIM* A338 (1994).