A Serializer ASIC at 5 Gbps for Detector Front-end Electronics Readout

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Abstract. Optical data links are used in detector front-end electronics readout systems of experiments in the Tevatron and the LHC. Optical links in high energy particle physics experiments usually have special requirements such as radiation tolerance, ultra high reliability and low power dissipation. These requirements are often not met by commercial components which are designed for applications in non-radiation, accessible (for maintenance) environment, and for multi-vendor systems so the parts must comply with certain standards. Future HEP experiments such as the upgrades for the sLHC call for optical links with ultra high data bandwidth, higher radiation tolerance and ultra low power dissipation. To meet these challenges and in particular those in the upgrade for the ATLAS Liquid Argon Calorimeter readout that calls for an optical link system of 100 Gbps for each front-end board, we adopted a full custom front-end electronics system design based on application specific integrated circuits. Reported here are the development and test results of two circuits: a 5 Gbps serializer and a 5 GHz phase locked loop, and a block diagram design for the 100 Gbps optical link.

1. Introduction

ATLAS Liquid Argon Calorimeter has 1524 front-end board (FEB) in its electronics readout system. Each FEB reads out 128 detector channels. Detector signals are amplified and split into two channels: the analog summation of detector layer information to build trigger towers for level 1 trigger, and shaping and digitization for precision energy measurements. In this channel, after a three gain shaper that works with a 12-bit ADC to cover the full dynamic range required by physics, signals are sampled at 40 MHz and stored in a switched capacitor array (SCA) awaiting level 1 trigger. Selected events are then digitized and formatted to be sent through a single channel optical link to the back-end electronics system for further processing [1, 2 and 3]. Because of the level 1 trigger selection, data rate over the fiber channel is 1.6 Gbps. A block diagram of this readout scheme is shown in figure 1a. A total of 11 ASICs and several commercial-off-the-shelf (COTS) components that are specially qualified to be radiation tolerant for this location in the ATLAS detector are used in the FEB, making a complex system that took a long development time [4]. This FEB is qualified for 10 years of operation at the LHC nominal luminosity of $10^{34}cm^{-2}s^{-1}$. Many of the COTS and ASIC technologies are obsolete making it impossible to upgrade this readout system adiabatically to meet a factor of 10 of luminosity increase (hence much higher radiation in the operation environment) in the sLHC. A new design will have to be adopted for the upgrade. A tentative FEB2 architecture, as depicted in figure 1b, streams data to the back-end electronic, greatly simplifies the front-end logic. The price to pay is mostly in the optical link and the back-end data processing.

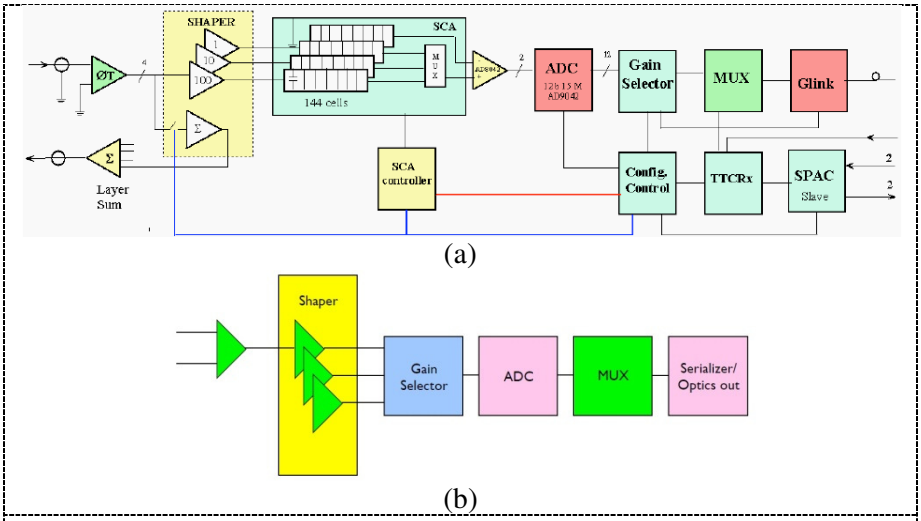

Figure 1. Block diagrams of the front-end board readout schematics of the current FEB (a), and the proposed upgrade FEB2 (b).

The Link-on-Chip (LOC) is a concept we proposed for the optical link upgrade which calls for a data bandwidth of 100 Gbps per FEB2, an increase of 62 times compared with the present system. The power dissipation of FEB2 is capped by the current cooling system that will not be upgraded, imposing a stringent power requirement on all ASICs for the front-end. We have identified an ASIC technology, a commercial 0.25 µm silicon-on-sapphire (SOS) CMOS process that meets the requirements on speed, power dissipation and radiation tolerance. A block diagram for the transmitting side of the link system is shown in figure 2. In this design a 6-lane serializer array called LOCs6 is the key component in the system. With a serializer data rate of 10 Gbps in each fiber channel, a 12-lane fiber ribbon will provide 100 Gbps data bandwidth plus 20% redundancy for system reliability. To check the serializer design, and to probe the highest speed possible with this technology, we submitted a prototype chip which we call SMU_P1. A picture of SMU_P1 is shown in figure 3. In this 3 mm × 3 mm tile, we have the following designs: LOCs1, a 5 Gbps 16:1 serializer; the LCPLL, a 5 GHz LC VCO based phase locked loop; The CML driver of LOCs1; A divide-by-16 circuit; A varactor, a voltage controlled capacitor; and an SRAM block, designed by INFN Milano.

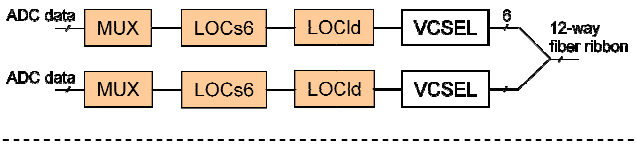

Figure 2. Block diagram for the transmitting side of the optical link upgrade to 100 Gbps per FEB.

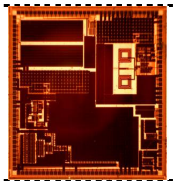

Figure 3. A picture of the SMU_P1 ASIC prototype.

SMU_P1 was submitted for fabrication in Aug. 2009. The chips arrived at SMU in Nov. 2009. Test setup was prepared during that time window. Test results of LOCs1 and the LCPLL are reported in section 2. A roadmap towards the 100 Gbps system is discussed in section 3.

2. Test results of LOCs1 and the LCPLL

Tests on the ASIC designs are in two categories: characteristic evaluations in lab and irradiation tests with a proton beam. Reported in this article are the former while results concerning the latter will be reported at TWEPP 2010.

2.1. LOCs1.

LOCs1 is a 16:1 serializer based on a 2.5 GHz ring oscillator PLL. Using both edges of the clock, a serializing unit is constructed with a design speed of 5 Gbps, as shown in figure 4. Working with the power of 2 enables us to use the CMOS 2:1 multplexing unit (MUX 2:1) before the last stage where we trade power for speed by using a multiplexer driven by a complementary clock. In the future design of the 10 Gbps serializer, a full CML multiplexer will be used at this stage.

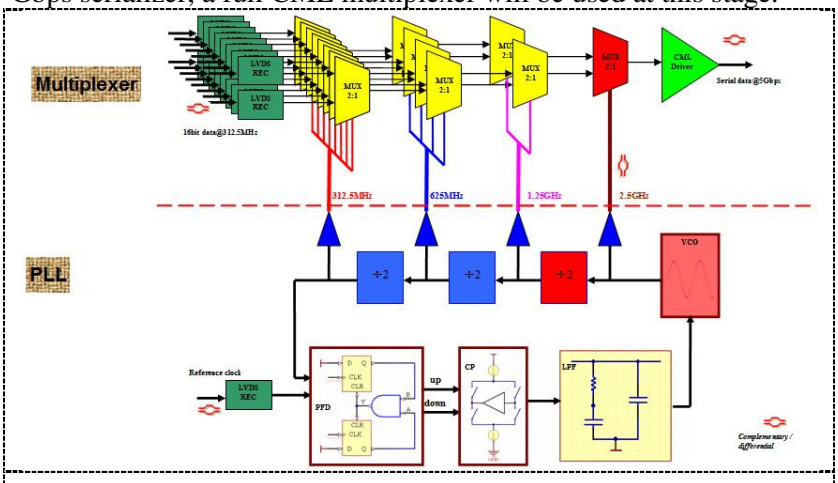

Figure 4. Block diagram of LOCs1.

There are two major measurements in the characteristic evaluations: the eye diagram and the eye mask test of the high speed output signal, and a stringent bit by bit check of the transmitted data in a bit-error-rate-tester (BERT), carried out in the form of the "bathtub scan" to measure the timing margin in the serial bit stream with a given error rate. To perform a BER test with LOCs1 under proton irradiation, a portable BERT has been developed in the ATLAS-CMS common project, the Versatile Link [5]. The VBERT, up to 4 channels in one FPGA, was successfully used in a recent irradiation test at the Indiana University Cyclotron Facility (IUCF) [6]. All tests are performed with an input data that generates a 2^7-1 pseudorandom bit stream. Shown in figure 5 is part of the test setup for LOCs1. A total of 12 carrier boards have been assembled.

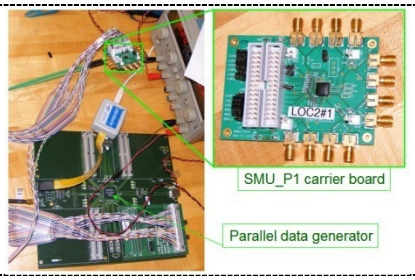

Figure 5. Pictures of part of the setup for testing LOCs1.

2.1.1. Eye diagram measurement and the eye mask test.

Eye diagram of the high speed output signal is measured to provide information on the rise and fall times of the signal, the amplitude and the timing jitter at the crossing pointing of the differential signal pair. An eye mask, adapted from Fiber Channel 4.25 standard and scaled up to 5 Gbps is imposed to the eye diagram which passes this eye mask test with a comfortable margin as shown in figure 6. Also shown in figure 6 is a simulated eye diagram with realistic output load to the last stage CML driver. As one can see, the measured eye diagram is slightly better than the simulated one, indicating that the conditions used in the simulation are conservative. The rise and fall times, signal amplitude and jitter are summarised in section *2.1.3*.

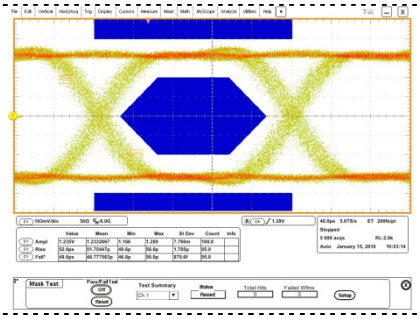

Figure 6a. The eye diagram measurement and eye mask test of LOCs1.

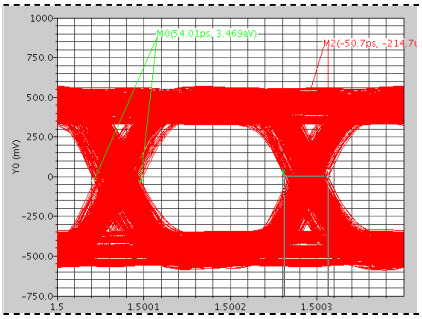

Figure 6b. The simulated eye diagram of LOCs1.

2.1.2. The bathtub scan.

Bathtub scans are performed at the design speed of 5 Gbps and at a higher speed of 5.8 Gbps. The results are shown in figure 7. At 5 Gbps there is an opening of 138 ps at a BER of 1×10^{-12}, comparable with the eye opening in the eye diagram measurement.

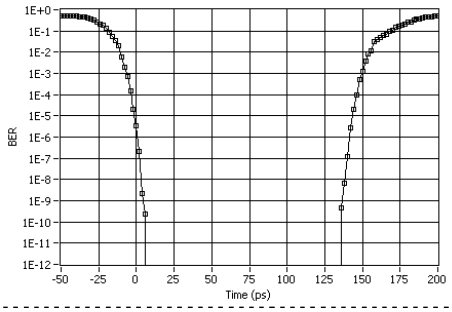

Figure 7a. Bathtub scan of LOCs1 at 5 Gbps.

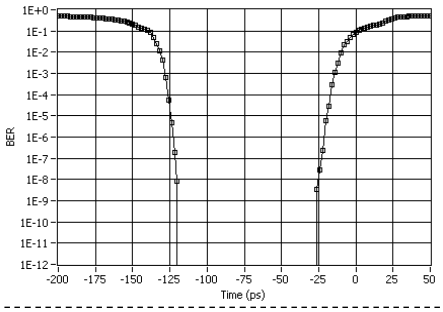

Figure 7b. Bathtub scan of LOCs1 at 5.8 Gbps.

2.1.3. Summary of LOCs1 test results.

A total of 12 LOCs1 were wire bonded to PCBs and tested. Five boards have problems: 2 Vcc shorts, 2 Vcc open, 1 with a stuck bit. They are all traced to the place where the chip is encapsulated, leaving unanswered questions to the problems: chip problems or wire bonding problems. Only tests on more chips will tell. For the 7 chips/PCBs that are working, the results are summarized below and in table 1.

- Range (Gbps): min: 3.8 – 4.0, max: 5.7 – 6.2.
- Power (based on 1 chip): 507 mW at 5 Gbps.

Table 1. Signal characteristics of LOCs1 at 5 Gbps

Amplitude (V)	1.16 ± 0.03
Rise time (ps)	52.0 ± 0.9
Fall time (ps)	51.9 ± 1.0
Random jitter (ps)	2.6 ± 0.6
Total deterministic jitter (ps)	33.4 ± 6.7
Total jitter at BER@1E-12 (ps)	61.6 ± 6.9
Eye opening at BER@1E-12	(69.3 ± 3.7)%
Bathtub curve opening at BER@1E-12 (ps)	122 ± 18

We consider the design goals of LOCs1 have been achieved.

2.2. The LCPLL

To reach a data bandwidth of 100 Gbps over a 10- or 12-lane fiber ribbon, we will need 8 to 10 Gbps transmission rate over a single fiber channel. The most crucial component in a serializer design is the PLL. In SMU_P1 we placed an LC based PLL design to work at 5 GHz. A block diagram of this PLL is shown in figure 8. The added CML driver is for test only.

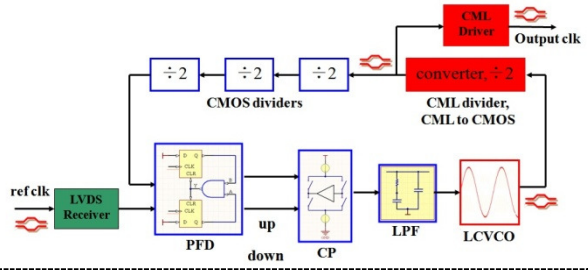

Figure 8. Block diagram of the LCPLL.

2.2.1. LCPLL measurement results

Four chips are measured and the results are listed in table 2. The tuning range of 4.7 to 5.0 GHz, although reaching the design goal of 5 GHz, is narrower than the simulated 3.8 to 5.0 GHz window. The power consumption of this PLL is 121 mW at 4.9 GHz, much lower than the ring oscillator based PLL used in LOCs1, which is 173 mW at 2.5 GHz, according to simulation.

Table 2. Parameters measured for the LCPLL

	Lower limit				Higher limit			
Board ID	1	2	3	4	1	2	3	4
Output frequency (GHz)	2.38	2.29	2.24	2.37	2.50	2.51	2.48	2.50
VCO frequency (GHz)	4.75	4.62	4.48	4.74	4.98	5.01	4.97	4.99
Rise time (ps)		66.2	47.0	67.1		67.2	42.1	66.1
Fall time (ps)		64.6	46.5	68.5		66.8	41.9	66.4
Random jitter RMS (ps)	1.28	2.49	2.05	1.81	1.26	1.06	1.08	1.83
Deterministic jitter (ps)	12.61	11.00	13.95	15.46	5.51	5.10	16.63	8.43

2.2.2. The narrow tuning range and the debugging

There two places that may cause the tuning range to reduce: the range of the varactor and the divider chain. Using the varactor in SMU_P1, we compared the measurement value against simulated values as shown in figure 9.

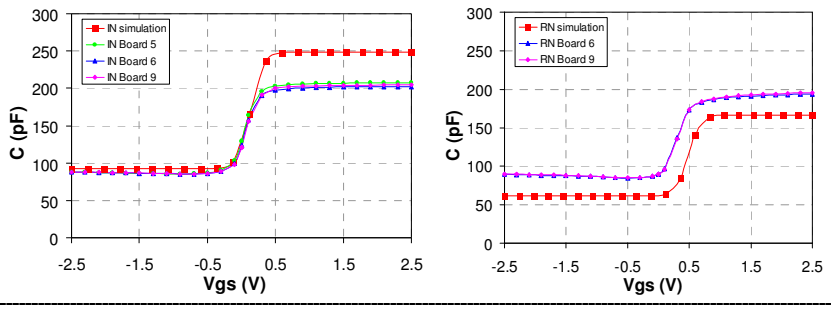

Figure 9. Varactor parameter measurements.

We use only RN type varators in the present design. Although there is a shift in absolute capacitance value, it is clear from the measurement that the tuning range should be the same as simulation.

Further investigation revealed a design mistake in the first stage divider that produces a glitch at low frequency end. This problem is understood and will be fixed in future designs.

3. Roadmap towards a 100 Gbps system

To achieve the required 100 Gbps per FEB data bandwidth for ATLAS LAr readout upgrade for the sLHC, the key development lies on the LOCs6 array serializer. A block diagram of LOCs6, together with the optical interface is shown in figure 10. A switch in the input data path provides a 20% redundancy for possible single channel failure. This design work is being carried out in the Department of Physics, Southern Methodist University.

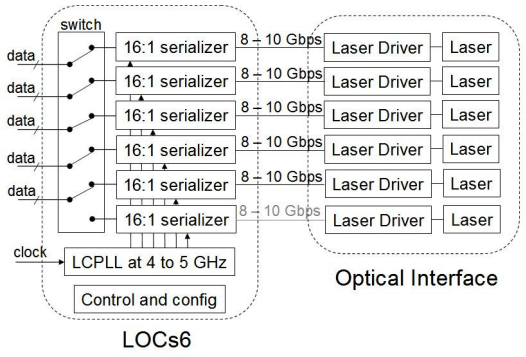

Figure 10. Block diagram of LOCs6 together with the optical interface.

We benefit from the ATLAS-CMS common project the Versatile Link on identification and irradiation evaluation on 10 Gbps lasers, fibers and passive components such as connectors and mechanical packages. We also adapt the system level specifications for optical links developed in the Versatile Link project.

Acknowledgements

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[5] For more information: https://espace.cern.ch/project-versatile-link/public/default.aspx

[6] For more information: http://www.iucf.indiana.edu/