A 16:1 serializer ASIC for data transmission at 5 Gbps

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ABSTRACT: A high speed, low power 16:1 serializer has been developed with a commercial 0.25 μm silicon-on-sapphire CMOS technology. The serializer operates from 4.0 to 5.7 Gbps. The total jitter is 62 ps and the eye opening of the bathtub curve is 122 ps at bit error rate of 10^{-12} at 5 Gbps. Power consumption is 463 mW at 5 Gbps. A proton beam test indicates the serializer is suitable for applications in high energy physics experiments.

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[1]On behalf of the ATLAS Liquid Argon Calorimeter Group.

Contents

1   Introducion

The optical data links for the ATLAS liquid argon (LAr) calorimeter between the front-end boards (FEBs) and the backend electronics operate at 1.6 gigabit per second (Gbps) per fiber channel [1]. In the ATLAS LAr calorimeter readout electronics upgrade for the sLHC, it is proposed to remove the analog Level-1 trigger sum from FEB and transmit continuously digitized data off the detector. Consequently, the data rate of the optical links increases from 1.6 Gbps to about 100 Gbps per FEB. The total data rate of 1524 FEBs reaches 150 Tbps [2]. However, the data rate of G-Link or GOL [3, 4] currently used in high energy physics experiments is 1.6 Gbps, too slow for the upgrade. Thus for the LAr calorimeter readout system, a high speed serializer working on detector is required. More than that, the running experiences of ATLAS experiment indicate that optical links in radiation environment are still fragile [5]. When an optical link carries multiple Gbps data stream, it is very important to improve the system reliability with redundancy.

A commercial $0.25\,\mu$m silicon-on-sapphire (SOS) CMOS technology has been evaluated to be suitable for the development of application specific integrated circuits (ASICs) for particle physics front-end readout systems. The thin silicon layer in this process significantly reduces the charge produced by passing particles and lowers the single-event effect (SEE) rate. The total ironizing dose (TID) is greatly reduced when the substrate is grounded [6, 7]. Based on the SOS CMOS technology we have developed a 5 Gbps 16:1 serializer, named as LOCs1. Cooperated with a 64/66 encoder, the serializer can provide close to 5 Gbps effective bandwidth. In this paper we present the design and test results of the serializer. We also present the initial design of a six-lane, 10 Gbps each lane serializer array with redundancy.

Figure 1. Block diagram of the serializer (left) and die micrograph (right).

2 Design

The serializer consists of a serializing unit, a phase lock loop (PLL) clock generator and a CML driver as shown in figure 1. The serializing unit multiplexes 16 bit parallel LVDS data into a serial bit stream. The serializer unit extends 2:1 multiplexers to a 16:1 one with binary tree architecture. Only the last 2:1 multiplexer needs to be optimized to work at the highest speed or 2.5 GHz. Two complimentary 2.5 GHz clock signals are required to speed up the D-flip-flop in the last 2:1 multiplexer. To achieve good immunity against the SEEs, we use large size transistors and static D-flip-flops in the whole design. With a 312.5 MHz reference clock input, the PLL clock generator provides 2.5 GHz, 1.25 GHz, 625 MHz, and 312.5 MHz clock signals to the serializing unit. A multiple-loop differential ring oscillator is used to boost the operating frequency of voltage control oscillator (VCO). The PLL loop bandwidth is programmable for adapting different reference clock qualities. The PLL can be configured to lock to either the rising or falling edge of the reference clock. This edge-selection feature is useful for the users to latch data with optimal timing. The CML driver can drive 50 Ω transmission lines.

The serializer occupies about 50% area of a 3×3 mm^2 die as shown in figure 1. All the I/O pins have electrostatic discharge (ESD) protection except the high speed serial data output pins.
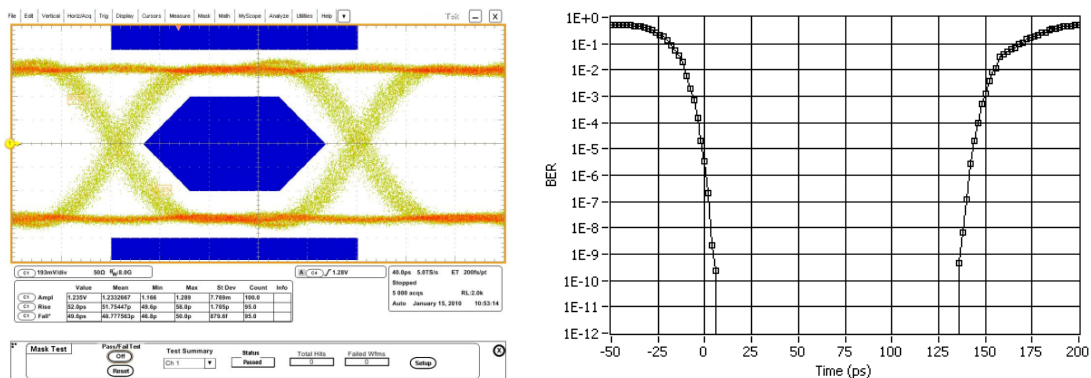
3 Test results

3.1 Test in laboratory

In the laboratory test, a field-programmable gate array (FPGA) based board provides 16 bit parallel data and a clock signal to a dedicated chip carrier board through a twisted pair cable. We measured the high speed serial data parameters through the SMA connectors on board with an oscilloscope and a bit error rate tester (BERT). Among the 12 assembled carrier boards, 7 boards work and the other 5 boards do not. Four carrier boards have power supply problems and one board has one stuck bit in the input data. We are going to investigate whether these problems are from ASIC fabrication or from wire bonding in the future.

We performed jitter measurements with $2^7 - 1$ pseudorandom binary sequence (PRBS) data pattern using oscilloscope software (Tektronix TDSJIT3). Using a commercial BERT (Anritsu

Table 1. Average values and standard deviation of the measured parameters of seven working boards.

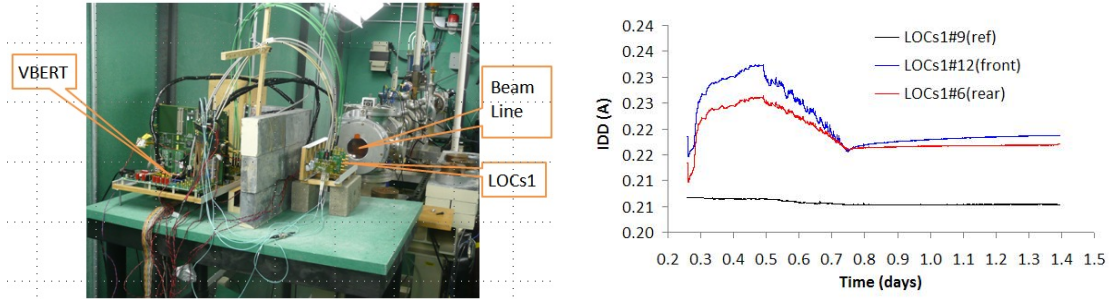|	
Output Amplitude (peak-peak, V)	1.16±0.03
Rise time (20%-80%, ps)	52.0±0.9
Fall time (20%-80%, ps)	51.9±1.0
Total jitter at BER of 10^{-12} (ps)	61.6±6.9
Random jitter (RMS, ps)	2.6±0.6
Deterministic jitter (peak-peak, ps)	33.4±6.7
Eye opening at BER of 10^{-12} (ps)	122±18
Power consumption (mW)	463±7
Upper working limit (Gbps)	4.0
Lower working limit (Gbps)	5.7

Figure 2. Eye diagram (left) and bathtub curve (right) at 5 Gbps.

Model MP1764C), we measured the bathtub curves. An eye diagram and a bathtub curve are shown in figure 2. The BER of all the seven boards are better than 10^{-12} in the data range from 4.0 to 5.7 Gbps. The parameters shown in table 1 are measured at 5 Gbps except the upper and lower working limit.

We also measured the jitter tolerance with a VBERT, a custom BERT [8]. During the measurements, LOCs1 is the serializer and an Altera Stratix II GX based board works as the deserializer and the error detector. With sinusoidal jitter injected at the reference clock of LOCs1, the measured jitter tolerance at BER of 10^{-12} and 5 Gbps is larger than 1.8 unit intervals (UI) when the injected jitter frequency is from 0.7 to 1.56 MHz. The measured jitter tolerance is larger than that specified in the Fibre Channel standard [9], suggesting that the link is robust and not sensitive to the reference clock jitter.

3.2 Radiation test

We performed a radiation test with a 200 MeV proton beam at Indiana University Cyclotron Facility. The test setup is shown in figure 3. The VBERT system for online error detection was placed in an area shielded by lead bricks. We put two LOCs1 carrier boards in the beam and another one

Figure 3. The radiation test setup (left) and power supply currents change during the test and during annealing time (right).

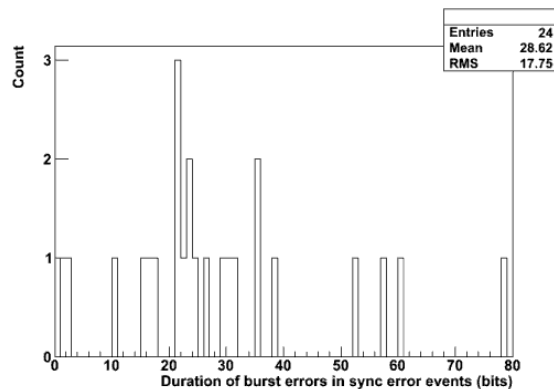**Table 2**. The observed number of single-event errors.

Board#	Number of single bit errors	Number of sync. Errors
6	0	16
12	5	8

in the shielded area as a reference. To test the possible angle effects, the angle between the beam incident direction and die surface normal was set at 0, 30, 45, or 60 degree during the radiation test. The boards accumulated 90% of the total fluence when their angles were kept at 60 degree. Because the number of the single-event upsets (SEUs) were small, we did not observe any statistically significant dependence on angles.
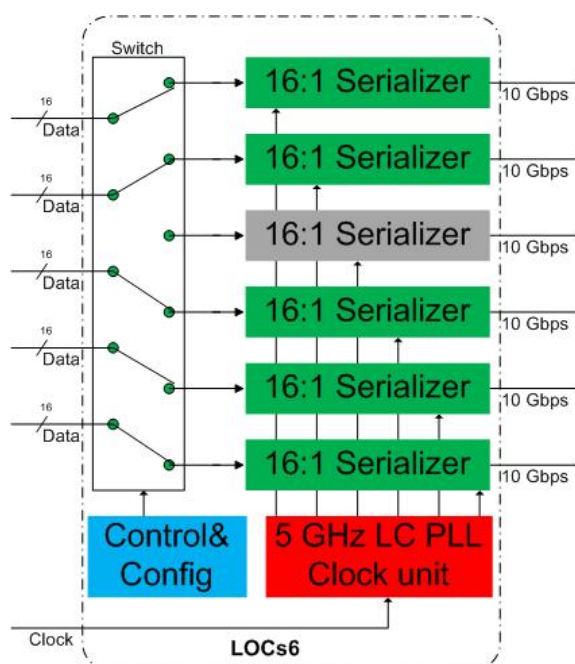
The test had lasted for 12 hours in the beam and we kept the test system running for 15 hours after the beam went off. We did not observe any bit errors in the annealing time. The LOCs1 power currents changed less than 6% during the beam time and annealing time. This means the TID effects are negligible for our application. We observed two types of SEUs: single bit errors and synchronization errors. The numbers of the observed SEUs are shown in table 2. We observed five single bit error events in total which did not affect the link status afterwards. The extrapolated BER for the single bit errors is 1.6×10^{-18} at sLHC ATLAS LAr calorimeter. When a synchronization error event occurred, there was a burst of bit errors occurring in a short duration. After the burst of bit errors, the received data stream consistently shifted one bit. The bit shift was removed when the receiver was reset for a word alignment. The duration distribution of the burst errors is shown in figure 4. Because the burst of bit errors lasts only several tens bits, for each synchronization error event, the link can be recovered on the receiver side without many bit loss. The extrapolated number of synchronization error events is less than 3 at the ATLAS LAr calorimeter in the whole sLHC life time.

4 Future work

To meet the challenge of 100 Gbps data rate per FEB, parallel optical links are studied. The parallel optical links use two 6-lane 10 Gbps serializer array chips and a 12-way fiber ribbon for each FEB. By adding a switch network on the input data path of the serializer array, one of the 6 serializers

Figure 4. The duration distribution of burst errors in synchronization error events.

Figure 5. The block diagram of 6-lane serializer array.

can be configured as a redundant channel to improve the optical link system reliability, as shown in figure 5. The serializer marked in grey color is configured as a redundant channel.

The critical component of the serializer array is a 10 Gbps serializer. By using the same architecture as shown in figure 1, the 5 GHz PLL clock unit, the clock buffer, the high speed divider, the last stage 2:1 multiplexer and the CML driver need to be redesigned. We have implemented a LC PLL on the same die as LOCs1 and the test results indicate that it can provide 5 GHz low jitter clock signal with low power consumption. The CML driver used in the LOCs1 is measured to be able to work up to 8.5 Gbps with no bit error. We plan to improve the bandwidth of the CML driver using the inductive peaking technology. The design of the CML buffer has started and the preliminary simulation results manifest that the approach is promising.

5 Conclusion

We have designed a 5 Gbps serializer for the ATLAS LAr calorimeter readout optical link upgrade based on a commercial SOS CMOS technology. The laboratory and radiation tests indicate that we have achieved our design goals. The 6-lane 10 Gbps serializer array is under development and the initial studies on several critical components are promising.

Acknowledgments

References

[1] N.J. Buchanan at al., *Design and implementation of the Front End Board for the readout of the ATLAS liquid argon calorimeters*, 2008 *JINST* **3** P03004.

[2] Arno Straessner, *Development of new readout electronics for the ATLAS LAr calorimeter at the sLHC*, in *Topical workshop on electronics in particle physics (TWEPP)*, Paris, France, 21-25 Sep. 2009.

[3] Manufactured by Hewlett Packard, Agilent Technologies, P.O. Box 10395, Palo Alto, CA 94303, http://www.datasheetcatalog.com/datasheets_pdf/H/D/M/P/HDMP-1022.shtml.

[4] P. Moreira1 et al., *A Radiation tolerant gigabit serializer for LHC data transmission 2001*, in *7th Workshop on Electronics for LHC Experiments*, 10–14 Sep 2001, Stockholm, Sweden, pp.145–149.

[5] T. Liu, *Optical Links for ATLAS liquid argon calorimeter front-end electronics readout*, in *Topical Workshop on Electronics for Particle Physics 2010*, 20–24 September 2010, Aachen, Germany.

[6] T. Liu et al, *Total ionization dose effects and single-event effects studies of a 0.25 um silicon-on-sapphire CMOS technology*, in *9th European Conference Radiation and Its Effects on Components and Systems (RADECS)*, Deauville, France, Sep. 2007.

[7] M. King et al, *Response of a commercial 0.25 μm thin-film silicon-on-sapphire CMOS technology to total ionizing dose*, in *Topical Workshop on Electronics for Particle Physics 2010*, 20–24 September 2010, Aachen, Germany.

[8] Annie Xiang et al., Design and verification of a bit error rate tester in Altera FPGA for optical link developments, in *Topical Workshop on Electronics for Particle Physics 2010*, 20–24 September 2010, Aachen, Germany.

[9] INCITS working draft proposed American National Standard for Information Technology, FIBRE CHANNEL Physical Interface-4 (FC-PI-4) REV 8.00, May 21, 2008