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Design and verification of an FPGA based bit error rate tester

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Abstract

Bit error rate (BER) is a principle measure of data transmission link performance. With the integration of high-speed transceivers inside a field programmable gate array (FPGA), the embedded solution provides a cheaper alternative to dedicated table top equipment and offers the flexibility of test customization and data analysis. This paper presents a BER tester implementation in the Altera Stratix II GX and IV GT development boards. Architecture of the tester is described. Lab test results and field test data analysis are discussed.

The Stratix II GX tester operates up to 5 Gbps and the Stratix IV GT tester operates up to 10 Gbps, both in 4 duplex channels. The tester deploys a pseudo random bit sequence (PRBS) generator and detector, a transceiver controller, an error FIFO logger and also includes a computer interface for data acquisition and user configuration. The tester's functionality is validated and performance is characterized in a point-to-point optical link setup. BER vs. receiver sensitivity is measured to emulate stressed signal conditions. The Stratix II GX tester is also used in a proton test on special designed serializer chips to record and analyse radiation induced errors.

Keywords: Front-end electronics, bit error rate, FPGA, optical link

1. Introduction

High speed links are widely deployed in the data acquisition systems (DAQ) designed for the next generation high energy physics (HEP) experiments. Data generated by detectors are to be transferred from the front-end electronics to the remote processing stations at high rate and accuracy with low latency. While copper offers design and integration flexibility at the short interconnect level, extended links are dominated by fiber optics. The read-out link design is a common task but often customized to deal with a

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unique set of requirements set by the different experiments. To characterize component, verify function and validate design, bit error rate (BER) performance are always evaluated in the laboratory and often times in radiation environments.

As a fundamental and efficient measure for high-speed transmission performance, BER tests are routinely carried out by table top equipment which is dedicated and expensive. When commercial FPGAs with embedded multi-gigabit per second transceivers emerge, it becomes sensible to implement an FPGA based BER tester with typical pattern generation, error detection function and data communication interfaces as a low cost and portable alternative to the stand-alone testers. As a reconfigurable device, FPGA-based BER tester is also much more flexible and can be customized to cater various test schemes and system protocols.

FPGA vendors always provide users with pre-designed IP cores that enable reconfigurable or embedded hardware. Various common functions and reference designs are also accessible. Function blocks are encapsulated and pluggable. For example, an 8B/10B encoder and decoder can be enabled or by-passed in the transceiver data path to emulate different system architects. For HEP data readout systems, it is important to understand how this and other communication protocols affect the transmission of event data as well as time, trigger and control information [1][2]. In term of data acquisition and error analysis, the support is much lacking probably due to the high level of dependence on specific tasks set by the individual tests.

We have implemented a custom BER tester based on Altera's Stratix II GX transceiver signal integrity development board. It was developed to demonstrate a point-to-point serial optical link with data rate up to 5 Gbps for LHC upgrade [3]. In this tester, we implement an error logging FIFO to record both bit error data and link status. The throughput of a PC accessing the FIFO data via USB port is also optimized. The tester's functionality is validated with a stand-alone BER tester. BER vs. receiver sensitivity is measured to emulate stressed signal conditions. The tester is also used in a proton test on custom serializer chips with real errors recorded and analysed. We then update the tester based on Stratix IV GT development board with Ethernet port to PC. Tests are performed up to 10 Gbps.

The next section presents the FPGA development boards as base platforms for tester implementation. The architecture of the BER tester and updates are specified in section 3 followed by the description of various test setups and measurement results in section 4. Finally a conclusion is given in section 5.

2. FPGA platforms

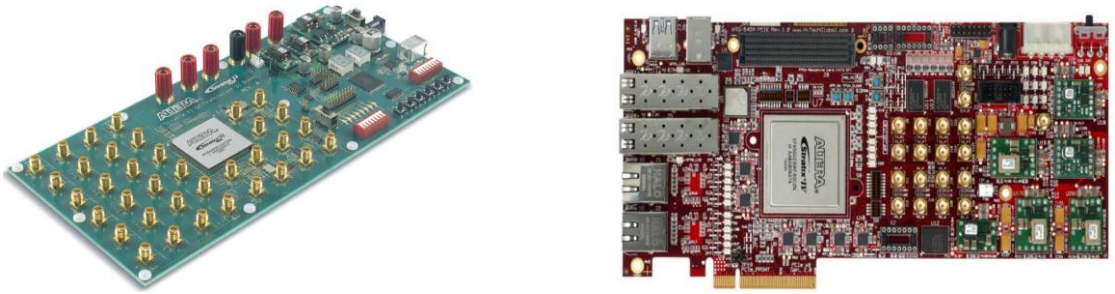
2.1. FPGA and development board hardware

The Altera FPGA with embedded transceivers was introduced in early 2000 with the Stratix II GX device family. The highest serial data rates increase from 6.375 Gbps in Stratix II GX to 11.3 Gbps in Stratix IV GT and now up to 28 Gbps in Stratix V GT. To balance cost and performance, we chose the Stratix II GX device to develop a system demonstrator for a point-to-point serial optical link with data rate up to 5 Gbps for the LHC upgrade. The Stratix II FPGA devices are available in production today, but the development board is updated to Stratix IV edition.

These embedded transceiver blocks implement dedicated hardware that can be configured to support many serial data communication standards including PCIe, SONET, Gigabit Ethernet etc. Common data path function blocks such as serializer/deserializer, boundary detector and rate matcher can be configured via pre-defined IP cores. For the targeted data offloading applications, standard communication protocols are neither efficient nor able to meet the timing requirements. Thus the transceivers are configured in basic mode. The data interfaces are adequate for BER tests at the physical layer while the data path architecture is transparent to custom protocol adaptation. Many mid-layer pluggable function blocks,

such as 8B/10B encoder/decoder, can be incorporated as options. The 8B/10B coding effect on error distribution was studied in the GX platform. In the GT platform, all mid-layer function blocks are disabled for the transceiver to run at the highest data rate of 11.3 Gbps. Functions such as word alignment need be implemented outside of the transceiver block in the FPGA main logic.

Development boards provide a versatile hardware platform for rapid prototyping projects. We used the Stratix II GX signal integrity development board from Altera as shown in figure 1(a) to demonstrate BER testing up to 5 Gbps and Stratix IV GT PCIe development board from HiTech Global as shown in figure 1(b) to demonstrate BER testing up to 10 Gbps. The Stratix II GX board features an EP2SGX90 device. Six full duplex transceiver channels at up to 6.375 Gbps each are wired to on-board SMA connectors. USB connection as serial port enables communicate with host PC. The Stratix IV GT board features an EP4S100G2 device. Twenty-four full duplex transceiver channels at up to 11.3 Gbps each are wired on board. Four channels go to SMA connectors and eight channels go to the high speed FMC (field programmable mezzanine card) connector for hosting custom modules. Two gigabit Ethernet ports are present for communication with host PC. Other interfaces include PCIe edge connector, USB3.0/2.0 hosts and SFP+ connectors.



(a) (b)

Fig. 1. (a) Stratix II GX development board; (b) Stratix IV GT development board.

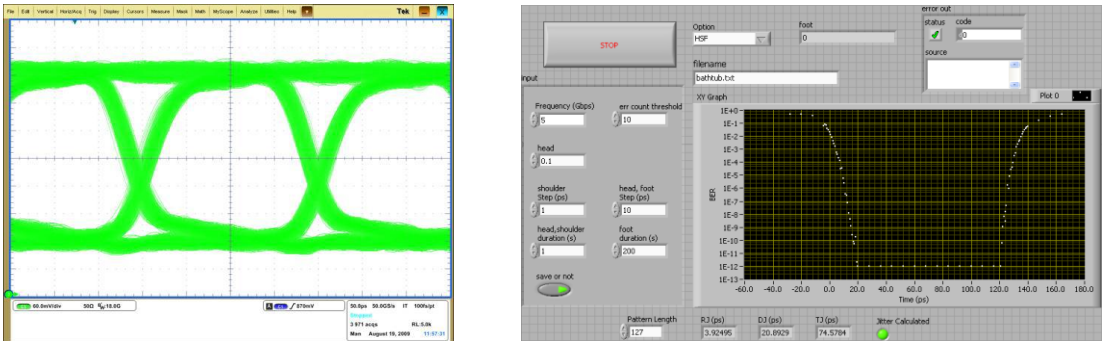
2.2. Transceiver characterization

To characterize the featured hardware we measured the transmitter output waveform. The eye diagram in figure 2(a) shows the electrical output of a Stratix II GX transmitter at 5 Gbps with zero pre-emphasis. It is complaint to industry standards such as 4G Fiber Channel and 10 Gigabit Ethernet scaled to 5 Gbps. This validates the use of the Stratix II GX transmitter to characterize downstream data link components. The eye diagram of the electrical output of a Stratix IV GT transmitter at 10 Gbps is also wide open. But higher bandwidth oscilloscope probes are needed for complete characterization.

The transmitter driven by random test patterns was tested by the receiver of a commercial stand-alone BER tester programmed to receive the same pattern. The resulted BER bathtub curve, i.e., BER measured against sample time scan from the left edge to the right edge of a data eye, provides necessary information to calculate the total jitter. The bathtub curve in figure 2(b) shows the electrical output of a Stratix II GX transmitter at 5 Gbps scanned. A total jitter of 0.225 UI (unit interval) or 45ps is measured, which is also standard compliant. Reference clock to the Stratix II GX transceiver is provided by an on board 156.25MHz oscillator and reference clock to the Stratix IV GT transceiver is provided by an external clock module board loading a 312.5MHz oscillator.

We compared the BER results of the Stratix II GX transceiver, the Stratix IV GT transceiver and a commercial stand-alone BER tester over the same optical link at 5 Gbps. The link BER vs. received

optical modulation amplitude (OMA) test setup will be discussed in detail in section 3. This test is also used to characterize the receiver sensitivity, the minimum optical power for achieving a specified bit error rate, i.e. at 10^{-12}. Receiver sensitivities of the same optical link measured by these testers are less than 1dB different, which is comparable to the measurement error floor.



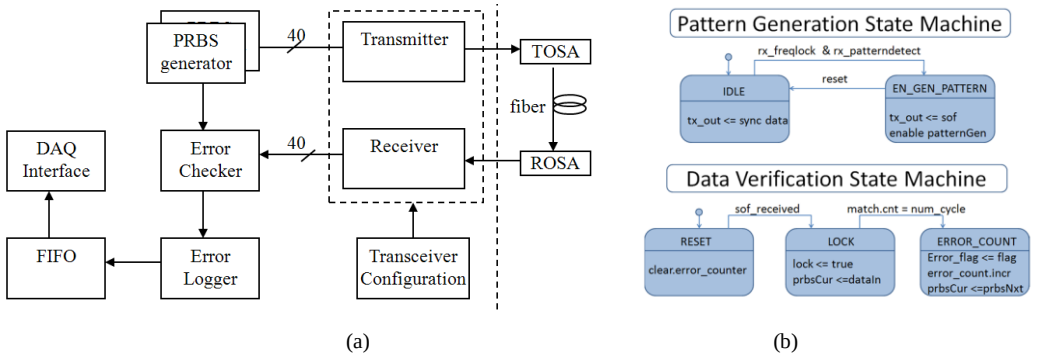
(a) (b)

Fig. 2. (a) Stratix II GX transmitter electrical output at 5 Gbps; (b) Stratix II GX transmitter scanned by a stand-along BERT receiver at 5 Gbps.

3. BERT architecture

The custom BER tester is an open source firmware and software package. The main blocks of the VHDL codes are pattern generator, error checker, transceiver core, error logger and user interface, as shown in figure 3(a). The LabVIEW routines includes USB and Ethernet library call, data acquisition and hardware configuration flow control, as well as programs for automated measurement.

Pseudo random bit sequence (PRBS) 7, 23 and 31 patterns are generated using parallel to serial implementation for low latency. The internal data bus is 40 bit wide so that the main FPGA logic can keep up with the serial transceiver. One of the benefits of PRBS is that long stress patterns can be produced without using a lot of memory. Another benefit of PRBS is that the patterns are time correlated, thus boundary synchronization is not necessary for BER testing. In the Stratix II GX tester, word aligner is integrated in the receiver data path. Pre-defined training patterns were thus transmitted and verified for



(a) (b)

Fig. 3. (a) block diagram of custom BER tester function blocks (including connections to an optical link); (b) state machine of the BER test structure.

the link to establish word boundary and for the state machine to advance to lock mode, as shown in figure 3(b). The error detector uses incoming data as seed to generate expected pattern in the lock state. After certain number of error free cycles, it switches to internal seed so that incoming erroneous bits cannot disturb the error checking of the detector. In the Stratix IV GT tester, word aligner need be removed for the transceiver to run at 10 Gbps. The training patterns are dismissed but since the PRBS can be verified without a set boundary, the tester will work with the rest of the process flow.

A FIFO is instantiated to communicate with external IO interface. The error logger monitors and records five types of events to the FIFO as shown in table 1. When link-lost events due to loss of signal or loss of clock occur, they are always logged in a reserved section of the FIFO. During the link lost event, bit error is not relevant and is no longer recorded. Instead the duration of the link-lost event can be derived when the link re-locks. More information from the error event can be retrieved from the recorded XOR pattern of the received and expected data given the time stamps since the pattern is a known PRBS.

A user interface block is provided to establish simple communication protocol with external IO chips, which is USB in bulk FIFO mode for the Stratix II GX tester and Ethernet in GMII mode for the Stratix IV GT tester.

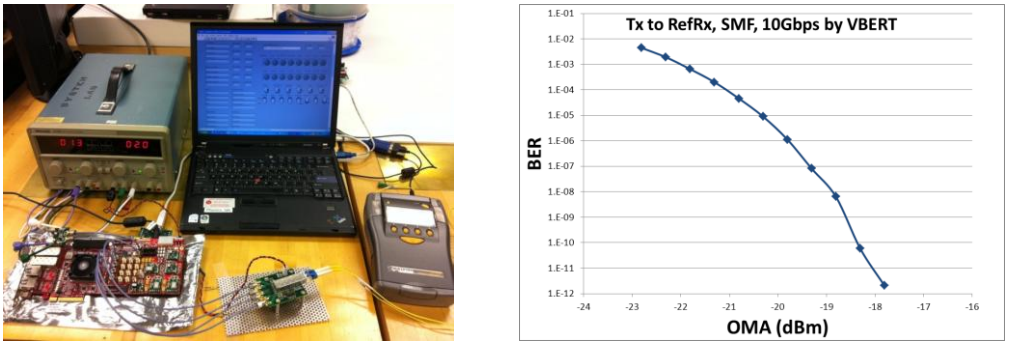
Table 1. Error FIFO data structure

Event	ID	Stamp	Data	Note
Single error event	001	yes, 48bit timer	IN XOR Exp'd	
Link locked	010	yes, 48bit timer	Exp'd	Error checker locked to generator
Link lost	011	yes, 48bit timer	Exp'd	Receiver CDR lost synchronization
FIFO full	100	yes, 48bit timer	Exp'd	Stop recording error events
FIFO ready	101	yes, 48bit timer	Exp'd	Resume recording error events

4. Test setup and results

4.1 In lab verification

The basic BER testing was performed on a point-to-point optical link. The tester's transmitter drove the transmitting side of an optical transceiver and the tester's receiver was connected to the receiving side of another optical transceiver. A variable optical attenuator (VOA) was inserted in the fiber loop to stress to induce transmission errors. Bit error rate is then measured at different attenuation levels. Figure 4(a) shows the setup where a Stratix IV GT board was connected to a PC and the transceivers were routed to and from an optical loop with VOA. In figure 4(b) we plot the BER vs. received optical modulation amplitude on the link at 10 Gbps. In the noise dominate region, this relationship follow the general trend of error function of Gaussian distribution, where discrepancies are attributed to system nonlinearities as power penalties. Receiver sensitivity of the reference link measured is about -17 dBm, comparable to what is listed in vendor specification, thus dismissing power penalty induced by the setup. Basic BER testing using the Stratix II GX board at 5 Gbps result a curve with similar trend but slightly improved sensitivity as expected.



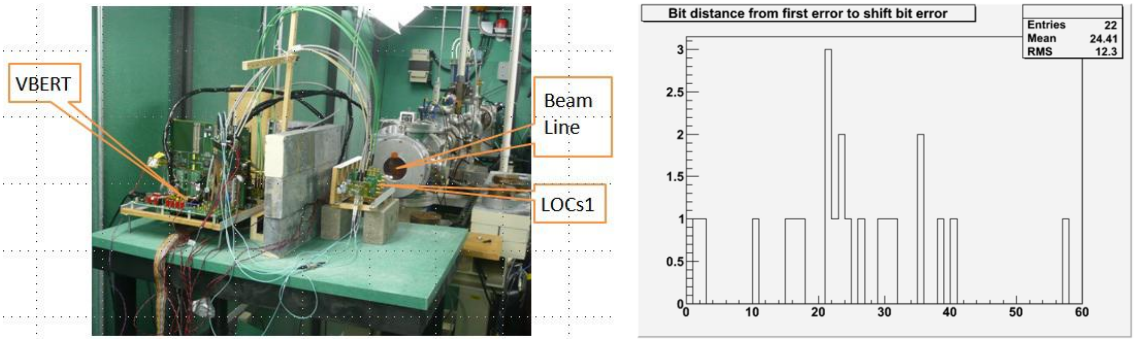
(a) (b)

Fig. 4. (a) Picture of Stratix IV GT tester routed to a point-to-point optical link; (b) Picture of Stratix II GX tester used in radiation test.

4.2 Radiation test application

The Stratix II GX tester was deployed in a radiation test on a 5 Gbps custom designed serializer chip with a 200 MeV proton beam at Indian University Cyclotron Facility. Figure 5(a) shows a picture of the setup where parallel PBRS data generated by a cyclone II FPGA were injected to the serializer and data output were feed to the Stratix II GX receivers. Two serializer boards were placed in the beam and the rest of the system in shielded area. When the flux reached the highest rate tested, a few errors occurred in both channels under radiation. We observed two types of single-event errors: single bit errors and synchronization errors. The single bit error events did not affect the link status afterwards, whereas the synchronization error required a receiver reset.

Post-test analysis of the error logging files showed that the synchronization errors result in exact one bit shift forward or backward, after a period of burst errors. The distribution of burst error lengths is shown in figure 5(b). The bursts are heterogeneous yet constrained within two data frames, i.e., 80 bits of serial transmission. For future reference, tester scheme like that of the Stratix IV GT where the detector lock does not depend on boundary alignment so that manual reset can be avoided is thus desirable for testing this type of devices.



(a) (b)

Fig. 5. (a) Optical link BER vs. received power; (b) Distribution of burst error lengths of synchronization error events

5. Conclusions

A custom bit error rate tester is developed to characterize and validate a serial optical link. The hardware platforms are the Stratix II GX development board operating up to 5 Gbps and the Stratix IV GT development board operating up to 10 Gbps. In addition to PRBS generator, detector and transceiver blocks, the error logger and user interface are implemented for data acquisition and targeted test analysis.

The tester is cross validated with stand-alone equipment. BER vs. receiver sensitivity of an optical link are measured. The tester is used in a proton test on custom serializer chips where two types of errors are recorded and analysed. A number of coding schemes and transmission protocols are experimented. These experience show the benefits of FPGA based BER tester in system prototyping and customization. Additional eight transceiver channels are to be extended to accommodate module cards with FMC connection on the Stratix IV GT platform.

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