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Installation and Commissioning of the ATLAS LAr Readout Electronics

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Abstract. The Liquid Argon Calorimeter (LAr) is a subsystem in the ATLAS experiment which is being assembled at the Large Hadron Collider (LHC) at CERN. The readout electronics system for the LAr is discussed here. The front-end of the readout will work in radiation environment. This special requirement has led to the development of a large number of rad-hard ASICs. The back-end of the readout employs DSPs to process data to reduce transmission bandwidth. The installation and commissioning of this readout is also discussed here.

Keywords: ATLAS, LHC, Liquid Argon, Readout Electronics, ASIC.
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INTRODUCTION

The ATLAS experiment [1] is designed to study the proton-proton collision from the LHC at a center-of-mass of 14 TeV to uncover and explore the physics behind the electroweak symmetry breaking. The Higgs searches through $H \rightarrow \gamma\gamma$ and $H \rightarrow 4$ *leptons* (here *leptons* = e,μ) and other new physics (ex.: $W' \rightarrow e\nu$, $Z' \rightarrow ee$) require efficient identifications, precision energy and spatial measurements of photons and electrons. SUSY searches using missing E_T require precision measurements of visible energies such as photons, leptons and jets. These requirements from physics dictate the design and construction of the ATLAS detector and its readout electronics.

The Liquid Argon Calorimeter (LAr) in ATLAS identifies photons and electrons and measures their energies. As shown in Figure 1, the LAr comprises three parts: the Electro-magnetic (EM) Accordion Calorimeter which forms the barrel part and the front portion of the endcap, the Hadronic End Cap Calorimeter (HCAL) and the Forward Calorimeter (FCAL). Together with the EM endcap part, the HCAL and the FCAL complete the endcap and the LAr has one barrel and two endcaps. This calorimter is almost hermetic: $|\eta| \leq 4.9$. The EM Accordion Calorimeter has a dynamic range from 20 MeV to 2 TeV to maximize the discovery potential, an energy resolution for photons and electrons designed to be $\sigma(E)/E(GeV) = 0.1/\sqrt{E} \oplus 0.007$. In order to achieve high spatial resolutions, the LAr has high granularity: about 195,000 readout cells. To match the detector performance, the readout electronics system has large channel numbers (195,000 channels), large dynamic (16 bits) range and excellenent linearity. The front-end of this readout situates on the detector and will be operated in radiation environment. This special requirement has led to the

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development of large number of rad-hard ASICs through various technologies available to different collaborating institutions in the LAr.

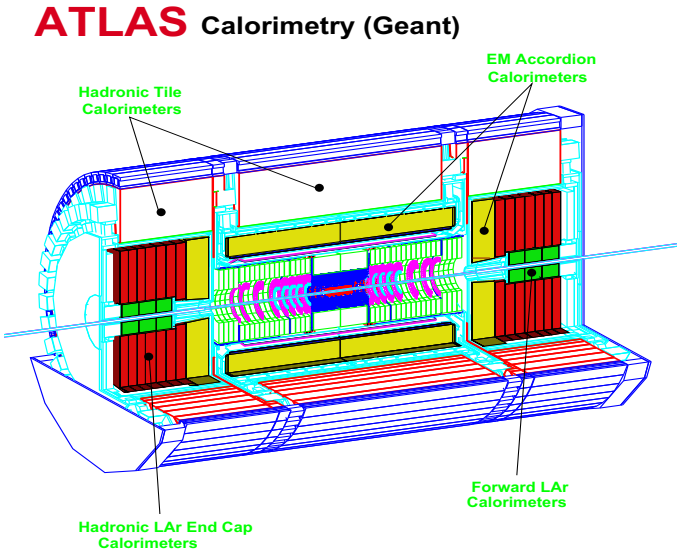

FIGURE 1. The ATLAS Calorimetry. Three parts compose the liquid argon calorimeter: the EM barrel and two endcaps. The EM barrel is placed in the barrel cryostat. The EM endcap, together with the HCAL and the FCAL fill the two endcap cryostats.

The ATLAS experiment is planned to be operational in year 2007. The LAr is being installed and will be commissioned through cosmic rays. In this note we will concentrate on the discussion of the LAr readout electronics system.

THE READOUT ELECTRONICS SYSTEM FOR THE LIQUID ARGON CALORIMTER

The LAr readout system is divided into two parts: the front-end and the back-end. The front-end electronics mounts on the detector and therefore has to withstand the radiation generated from the proton-proton collisions. The back-end receives data from the front-end, process them using a farm of 720 MHz digital signal processors (DSPs) to reduce the transmission bandwidth. Shown in Figure 2 is the block diagram of the LAr readout system. In the front-end crate, there are 28 FEBs (most cases). Each FEB reads out 128 detector channels. These FEB boards are calibrated by the Calibration Board which generates the calibration pulses through a 16 bit digital-to-analog signal converter. The Tower Builder Board (TBB) collects analog signals from each FEB and constructs energy deposition towers to provide the Level 1 trigger with information necessary to trigger the events. The trigger information comes back to the Controller Board in the front-end crate through the TTC fiber, together with the LHC clock that is used to clock the FEB. Triggered events are digitized on the FEB through a 12 bit ADC and are sent to the back-end electronics through a dedicated fast optical data link that operates at 1.6 Gbps serial data rate. In the back-end crate, the FEB data

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arrive at a board called the Read Out Driver (ROD) that collects data from 8 FEBs. On the ROD there are the 720 MHz DSP based processing units (PU) that process them and send the processed data to later stage electronics via the CERN developed Slink.

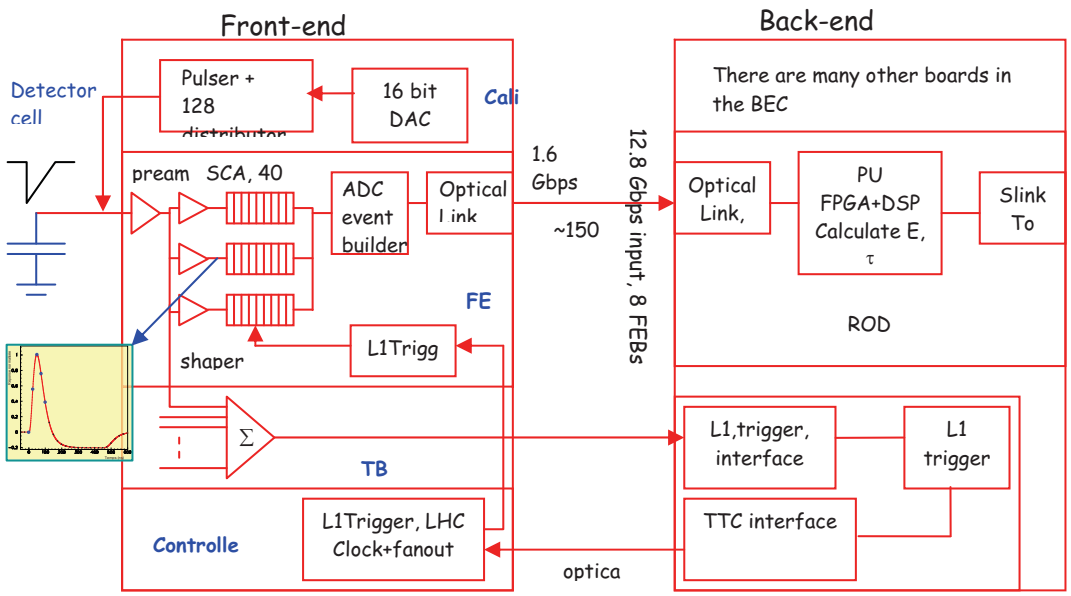

FIGURE 2. The ATLAS Liquid Argon Calorimeter readout electronics system block diagram.

Shown in Figure 3 is the more detailed block diagram of the FEB board.

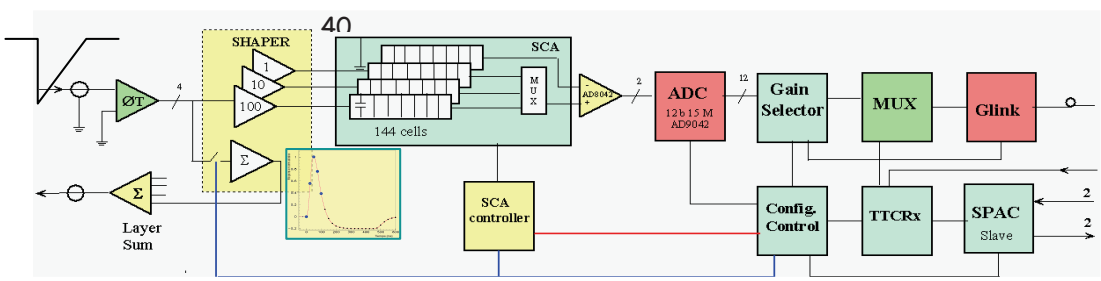

FIGURE 3. The FEB block diagram.

The detector cell generates a negative triangular current pulse from the energy deposition of a passing particle. This signal is amplified and shaped into a bipolar signal to eliminate electronics pileups. This signal is then sampled at 40 mega-sample per second (Msps) and stored in an analog memory (the SCA) waiting for the Level 1 trigger. Once triggered, the event stored in the SCA is sent to the analog to digital converter (ADC) to be converted into digital data format. Typically five samples around the positive peak of the bipolar signal are converted. Optimum Filtering method is used to obtain the peak amplitude which is proportional to the energy deposited in the detector cell. There are three gains from the shaper which amplifies the signal by factors of 1, 10 and 100. There is a gain selection mechanism built in the FEB to select the proper gain. Together with this gain selection and the 12 bit ADC, a

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16 bit resolution is achieved. A Glink chip based optical data link for each FEB converts the data from the ADCs into a 1.6 Gbps serial data stream and sends the data through a 50 micron core graded-index (GRIN) fiber to the ROD which sits in the back-end crate. Shown in Figure 4 is a picture of the top side of the FEB with its key components labeled.

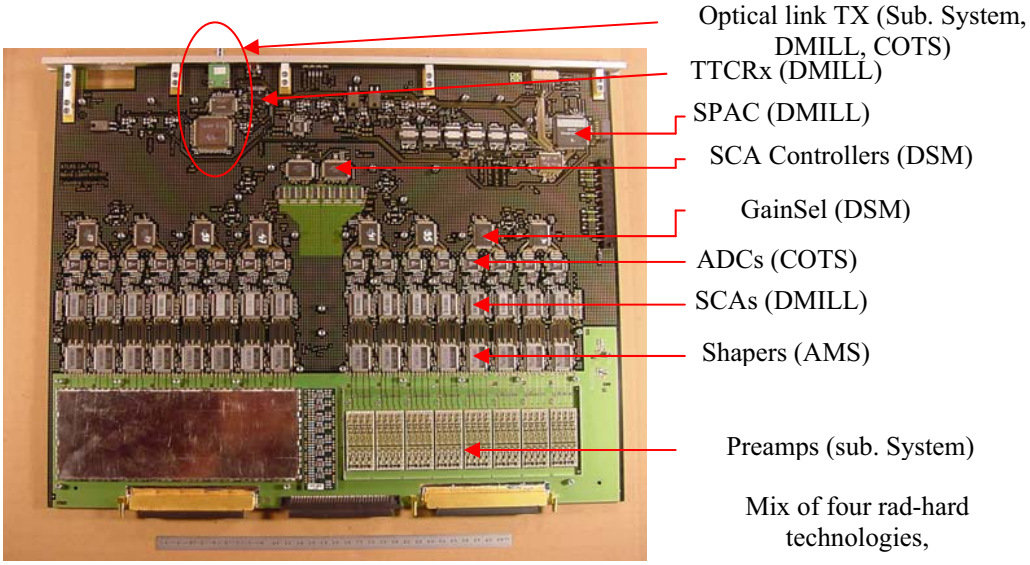

FIGURE 4. A picture of the front-end-board (FEB) and the key components on it. All components on the FEB have to be rad-hard. Four rad-hard ASIC technologies have been used to produce ASICs , The COTS on the FEB have been verified to be rad-hard.

The back-end system consists of several boards. Of them the ROD is the most important and complicated one. The block diagram of the ROD in the back-end is shown in Figure 5. A picture of the ROD and the PU that plugs onto the ROD is shown in Figure 6.

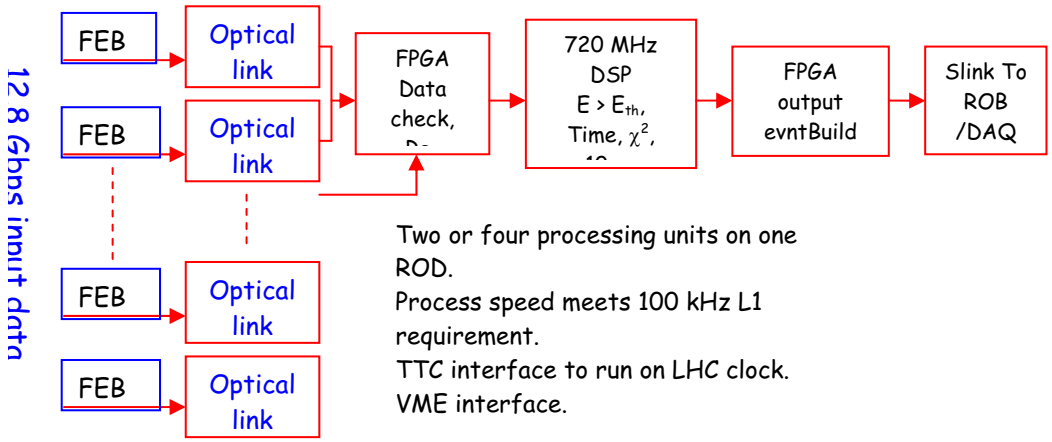

FIGURE 5. Block diagram for ROD in the back-end.

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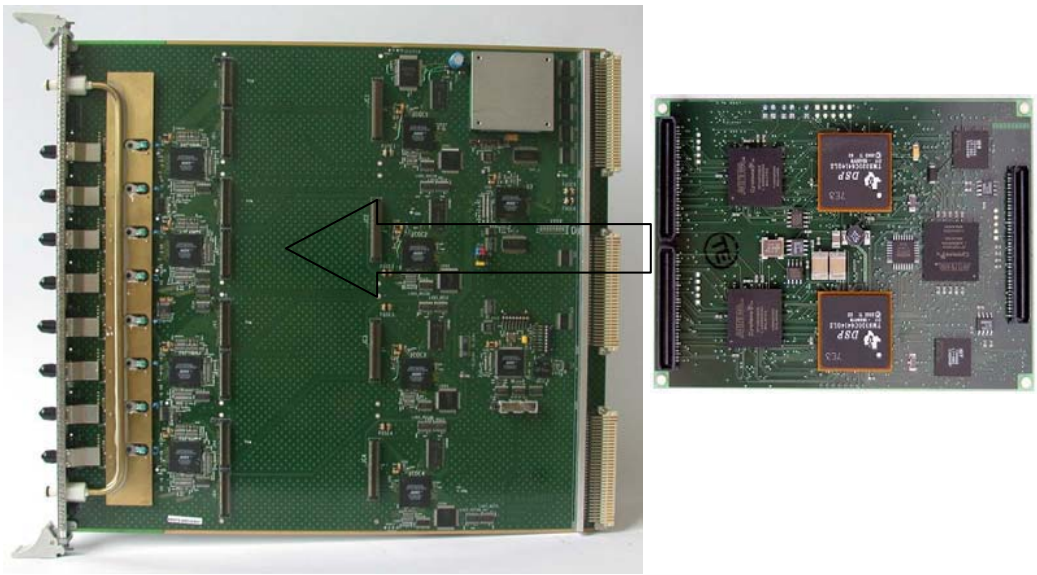

FIGURE 6. A picture of the ROD mother board and the PU that plugs onto it.

The ROD input data bandwidth is 12.8 Gbps, realized with 8 fibers carrying data from 8 FEBs. The data are preprocessed by FPGA chips. After this stage, the data are sent to the PU to be processed by the DSPs. Energy and other quantities, together with histograms are obtained by the DSPs. The energy is calculated using the Optimum Filtering method. Events with energy above a set threshold are sent to the output FPGA and then further shipped off the ROD through the Slink to a later stage in the data acquisition system.

THE DESIGN AND PRODUCTION CHALLENGES FOR THE LAR READOUT ELECTRONICS SYSTEM

The design challenges in the LAr readout system are mostly in the front-end, especially on the FEB, hence it is used as an example here. Once installed and commissioned, there will be very little access to these boards, so reliability becomes a serious issue because maintenance of these boards will only be possible during long period of LHC machine shutdowns. Each FEB reads out 128 detector channels, with 1524 FEBs to cover more than 195,000 detector channels. Although each readout channel consumes only 0.8W on the FEB, one FEB dissipates about 100 W in operation. Highly densely packed in the front-end crate, the FEBs are water cooled. Large 16 bit readout dynamic range dictated by physics is realized by a 12 bit ADC with 3 gains in the amplification/shaping channel. The analog signals are sampled at 40 MHz with 5 samples per pulse. The sampled data are stored in the SCA for Level 1 trigger latency of up to 2.5 μs, or 100 bunch crossings. The digitization of triggered event is carried out on the FEB, meeting the requirement of 100 KHz Level 1 trigger rate. After the digitization, events are sent off the FEB through an optical data link running at 1.6 Gbps serial data rate. The optical data link is used to reduce the

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coherent noise. The fact that there are small analog signals together with MHz to GHz digital signals on the same PCB makes the design and layout of the FEB very difficult. High speed serial data transmission requires ultra low clock jitter. In the case of the 1.6 Gbps optical link on the FEB, the clock jitter is required to be less than 20 ps. The clock jitter from the 40 MHz LHC clock distribution system is about 1 ns. Special rad-hard clock jitter cleaning circuit developed by CERN is employed on the FEB and an average of 10 ps clock jitter is achieved.

The boards in the front-end crate have to withstand radiation of over 10 years of LHC operation, estimated to be 50 Gy of ionizing radiation and 10^{12} n_{eq}/cm^2 of hadronic radiation. This requirement has led to a large number of rad-hard ASIC development and extensive rad-hardness evaluations of both ASICs and COTS. Listed in Table 1 are the ASICs developed for the FEB.

TABLE 1. ASIC development for the FEB

Technologies	Components	Number used in one FEB
AMS BiCMOS	Shaper	32
DMILL	SCA	32
	SMUX	1
	TTCrx	1
	CFGCTRL	1
	SPAC slave	1
Deep sub micron (0.25 μm)	GainSele	8
	QPLL	1
	CLKFO	1
	SCAC	2
	DCU2	2
RHBip 1	VREG	19

Production challenges lie in component, system integration and final FEB assembly levels. Example of the component level is the OTx, the electrical to optical signal converter that is used in the optical data link. The OTx is a custom designed subassembly that is 100% screened for quality assurance (QA) [2]. Since only 2000 OTx are produced, we do not have the luxury to have a preproduction of a few thousand modules to debug the production procedure. Problems in the production are actually solved during these QA measurements. The optical data link has been developed as a subsystem in lab before it is integrated onto the FEB. In a stand alone mode, the link is clocked by a crystal based oscillator which has a very small jitter. During the integration, jitter from the system clock is found not suitable for high speed serial data transmission. A special click jitter cleaning circuit has to be developed to cope with this problem and that is the QPLL chip from CERN, introduced to the FEB at a rather late stage in its development. The FEB itself is subject to a Highly Accelerated Stress Screening (HASS) during production. The HASS consists of heating and cooling cycles over 6 hours, simulating the first few weeks of LHC operation. This is designed to find problems in an early stage (the "infant mortality" due to problems in production and weak components). Component level and circuit level problems (ex: OTx and QPLL stability) were identified during early stage in the FEB production and were fixed. The FEBs are then tested at collaborating institutions

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for the full digital and analog functionality to assure that each FEB produced meets its design specifications.

INSTALLATION AND COMMISSIONING STATUS

The LAr readout system has been tested together with detector modules in beam tests. Shown in Figure 7 are preliminary results of electrons at 20 GeV and 180 GeV from beam tests, indicating that the detector and its readout system are working although the absolute calibration is off by a few GeV.

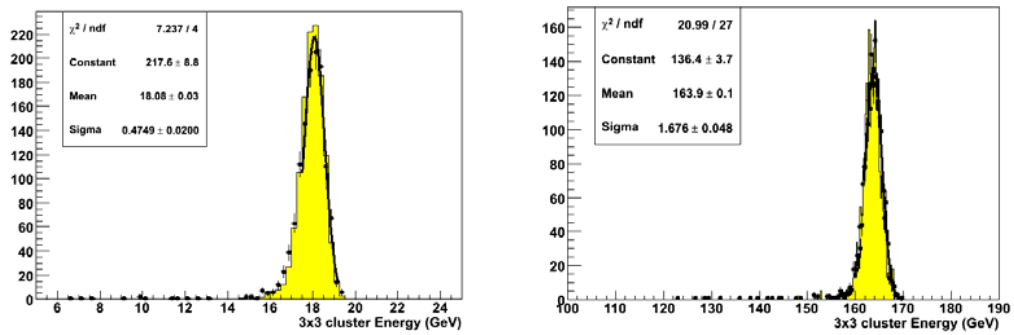

FIGURE 7. Preliminary results on electrons from beam tests indicating that the LAr detector and its readout system work.

The installation of the LAr detector and its readout electronics is taking place now. At time of the conference, the EM barrel front-end crates were fully equipped and tested. Endcap front-end crates were just started to be equipped. There was a lot of work on cabling, fiber splicing, cooling and other services taking placing in the ATLAS experimental hall. Back-end electronics installation matched well with the front-end. The commissioning of the detector with its readout system will be carried out later part of the year with cosmic rays.

CONCLUSIONS

The readout electronics system for the ATLAS LAr calorimeter is discussed in this note. The radiation environment in which the front-end electronics will be running imposes special rad-hard requirement for its components that has led to the development of a large number of rad-hard ASICs and lengthy evaluation of them, together with other COTS that are identified to be rad-hard and are used on the front-end electronics boards. This readout electronics system has been produced, tested in beam tests, and installed onto the ATLAS detector. A great deal of experience has been gain in component production, system integration and final board level assembly. The commissioning of the system together with the detector using cosmic rays is being carried out. This is a crucial step to ensure that the ATLAS experiment will be ready for the LHC colliding beam.

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