# Total Ionization Dose Effects and Single-Event Effects Studies Of a 0.25 μm Silicon-On-Sapphire CMOS Technology

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*Abstract*— **A test chip with various test structures has been designed and fabricated in a 0.25 μm Silicon-On-Sapphire CMOS technology and irradiated with a Co-60 gamma source and a 230 MeV proton beam. The sapphire substrate is left either floating or tied to ground when the transistors are irradiated with the Co-60 gamma irradiation up to 100 krad(Si). When the sapphire substrate is floating during irradiation, a radiation-induced leakage current increases in NMOS transistors at a low dose of 33 krad(Si) and in PMOS transistors at a high dose of 86 krad(Si). When the sapphire substrate is tied to ground during irradiation, the overall radiation-induced leakage current change for both NMOS and PMOS transistors is negligible. The radiation-induced threshold voltage shift for both NMOS and PMOS transistors quickly saturates with the total dose and stays unchanged. All the four types of shift register and latch chain test structures have exhibited single event effect immunity up to the fluence of 1.8×10$^{12}$ proton/cm$^2$. Our studies show that this technology is suitable for applications with total dose up to 100 krad(Si) and with a fluence up to 1.8×10$^{12}$ proton/cm$^2$.**

***Index Terms*—Application specific integrated circuits, CMOS integrated circuits, radiation effects, silicon-on-sapphire**

## I. Introduction

Silicon-on-Sapphire (SOS) CMOS technology has been used in applications for radiation tolerant electronics since 1970s. With the insulating sapphire substrate, this technology eliminates the parasitic bipolar junction transistors in the bulk silicon substrate and hence removes the mechanism for latch-ups. It has been reported to have smaller single event upset (SEU) cross sections than the bulk CMOS [1, 2]. However, the total ionization dose (TID) effects are usually of a concern because the SOS technology, like any Silicon-On-Insulator technologies, has radiation induced back channel leakage [3, 4] that is usually controlled through special fabrication process. In addition to the back channel, there is radiation induced edge leakage that is common to bulk CMOS and is usually mitigated through special layout techniques.

Historically, SOS technology was limited by low fabrication yields to very specialized applications in military and space programs. Peregrine Semiconductor Cooperation's UltraCMOS™ process [5] overcomes this problem, making the SOS technology available through MOSIS. Previous tests showed that the 0.5 μm UltraCMOS™ with special radiation hardening treatment can withstand radiation up to a few hundreds of krad(Si) [6].

Peregrine introduced recently its 0.25 μm UltraCMOS™ process. We are exploring the applicability of this process for the front-end readout Application specific integrated circuits (ASICs) in the optical link systems for the ATLAS [7] upgrade at the Large Hadron Collider [8]. A test chip with various test structures was designed and fabricated. The chip was irradiated with a Co-60 gamma source for TID effect studies and with a 230 MeV proton beam for the single event effect (SEE) study. Reported here are the TID results with a total dose of 100 krad(Si) and the SEE results with fluence of 1.8×10$^{12}$ proton/cm$^2$.

The test chip and the experimental setups are described in section II. Detailed TID studies are discussed in section III. Our results show that with a grounded sapphire substrate, the overall radiation induced leakage current increase becomes negligible. The threshold voltage shifts due to radiation for both NMOS and PMOS transistors quickly saturate and stay unchanged through out the irradiation. The results of the SEE study are presented in section IV. The technology demonstrates good TID tolerance with Co-60 gamma source and SEE immunity for 230 MeV protons as incident particles. We provide conclusions of this study in section V.

## II. The 0.25 μm UltraCMOS™ SOS Test Chip and the Experimental Setups

The basic features of the 0.25 μm UltraCMOS™ SOS technology used in the test chip are given in Table 1.

The chip contains an 8×12 array of transistors with different type (NMOS and PMOS), different channel widths (80 and 40 μm), and lengths (0.25, 0.5, and 1.0 μm), implemented in four different types of layout: 4-finger, 8-finger, and 16-finger

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standard layout, and the enclosed-layout transistors (ELTs) [9]. The gate terminals of all the transistors in the same row are connected together to save the chip pads. So do the source terminals of all the transistors in the same row and the drain terminals of all the transistors in the same column. The transistors in the same column share a drain terminal. The ELT and multi-finger transistors are used to separate the edge leakage currents from the back channel since the ELTs have no the edge leakage. Transistors of each particular type, size, and layout have three identical copies. They are spread out in the transistor array for better measurement statistics. A picture of this chip with functional blocks marked out is shown in Fig. 1.

Table 1. The technology features of the test chip

| | |
|---|---|
| VDD | 2.5V |
| Gate oxide thickness | 6 nm |
| Process | 0.25 μm SoS CMOS |
| Device isolation | LOCOS |
| Interconnectivity | 3 metal layers |
| NMOS polysilicon gates doping | N+ |
| PMOS polysilicon gates doping | P+ |

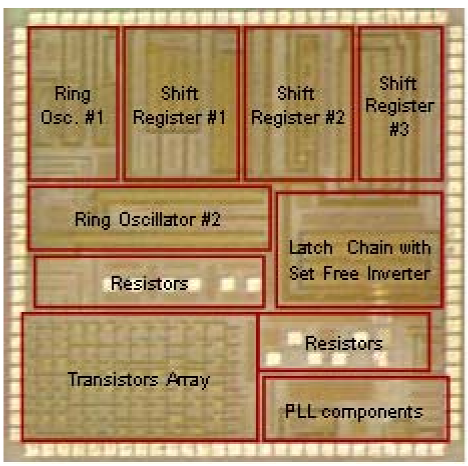


Fig. 1: Photograph of the SOS test chip.

The characteristic I-V curve of each transistor was measured using a picoammeter and three programmable DC power supplies. When the measurement range of the picoammeter (Keithley 6485) was changed, over ten-volt transition spike might appear on its input terminal and damage the transistor under test. Therefore, we chose the fixed measurement range from 10 nA to 2 mA. This limited the current measurement resolution to 25 nA (RMS). A reed relay switch array controlled by a USB DIO card was used to connect the terminals of the transistor under test to the picoammeter and the DC power supplies. The current through the drain ($I_D$) was measured as a function of the voltage between the gate and the source ($V_{GS}$) before and after the radiation while the voltage between the drain and the source ($V_{DS}$) was fixed at 0.1V for NMOS and –0.1V for PMOS. The $V_{GS}$ was swept between 0 and 1.5V when NMOS transistors were measured and between -1.5 and 0V in the PMOS case. When one transistor was measured, all other transistors in neither the same row nor the same column as the one under measurement were biased into an OFF state by connecting the source and gate terminals together with a 10-kΩ resistors and leaving the drain terminal floating. The transistors in the same row as the one under measurement had the same $V_{GS}$ and a floating drain terminal. The transistors in the same column as the one under measurement had the gate and source terminals connected with a 10-kΩ resistor and floating.

We used two different test conditions. In the first condition, during the irradiation the sapphire substrate was left floating with the transistors biased in the following conditions: $V_{DS}$ = 2.5 V and $V_{GS}$ = 0 V for NMOS, $V_{DS}$ = -2.5 V and $V_{GS}$ = 0 V for PMOS. The I-V curves were measured before and after the irradiation. In the second condition, the substrate was tied to ground during the irradiation. The I-V curves were measured continuously one by one during the irradiation.

More than 20 chips were irradiated with a Co-60 gamma source up to 100 krad(Si) followed by annealing studies at room temperature. Two main parameters, leakage current and threshold voltage, were extracted from the I-V curves. We chose the current at $V_{GS}$ = 0 V as the leakage current. The threshold voltage was extracted by using the method given in [10].

On the test chip, we designed three types of shift registers made up of standard geometry transistors, enclosed layout transistors, and resistively hardened cells [11] with standard geometry transistors respectively. Each type of shift registers is comprised of 32 stages of D flip flops (DFF) connected in a chain format. The sizes of both the PMOS and NMOS transistors in these shift registers are kept consistent for comparison purposes. The resistively hardened shift registers are divided into eight subsections. Each subsection has a resistor that doubles its value in the previous subsection. The resistor values are 1, 2, 4, 8, 16, 32, 64, and 128 kΩ. The resistors are placed in the output and feedback paths of the DFF to slow the response between nodes so that the circuit itself does not have time to respond to the radiation induced single event effects.

We designed a chain of latches based on single event transition (SET) free logic [12]. The idea for SET free logic is to construct logic elements that will not allow single event transients to generate and thus propagate to the outputs.

To accomplish the online test, a pseudo random bit stream (PRBS) was continuously written into each test shift register chain at 40 Mb/s via an FPGA. The bit stream was then read back to check for errors. For the resistively hardened latches, PRBS data was written in at a rate of 40 Mb/s. The data was then stored inside the circuit for a period of one second. Afterwards, it was read back into the FPGA to check for errors. In addition, we monitored current consumption of all test elements with a multi-channel digital multimeter.

The chip also contains ring oscillators, resistors, current mirrors, digital standard cells (NOT, NAND, and NOR), and the phase locked loop (PLL) components (divider, phase frequency detector, and voltage controlled oscillator). Their test is beyond the scope of this paper.

## III. STUDIES ON THE TOTAL IONIZATION DOSE EFFECT WITH CO-60

### *A. Sapphire substrate floating*

Shown in Fig. 2 are the I-V curves of NMOS (Fig. 2(a)) and PMOS (Fig. 2(b)) ELTs (W/L = 40 µm/0.25 µm) before and immediately after the irradiation at two different total doses with the same dose rate of 0.33 rad/s. As can be seen in the I-V curves of NMOS transistors, the threshold voltage ($V_{TH}$) decreases 80 mV and the leakage current increases from less than 100 nA to 2.3 µA at the low dose of 33 krad(Si). The threshold voltage increases 200 mV and the leakage current stays the same in the measurement error range as before irradiation at the high dose of 86 krad(Si). In contrast to the NMOS case, from the I-V curves of PMOS transistors, we observe that the threshold voltage and the leakage current stay unchanged at the low doses of 33 krad(Si). The absolute value of the threshold voltage ($|V_{TH}|$) decreases 180 mV whereas the leakage current increases from less than 100 nA to 2.7 µA at a high dose of 86 krad(Si)).

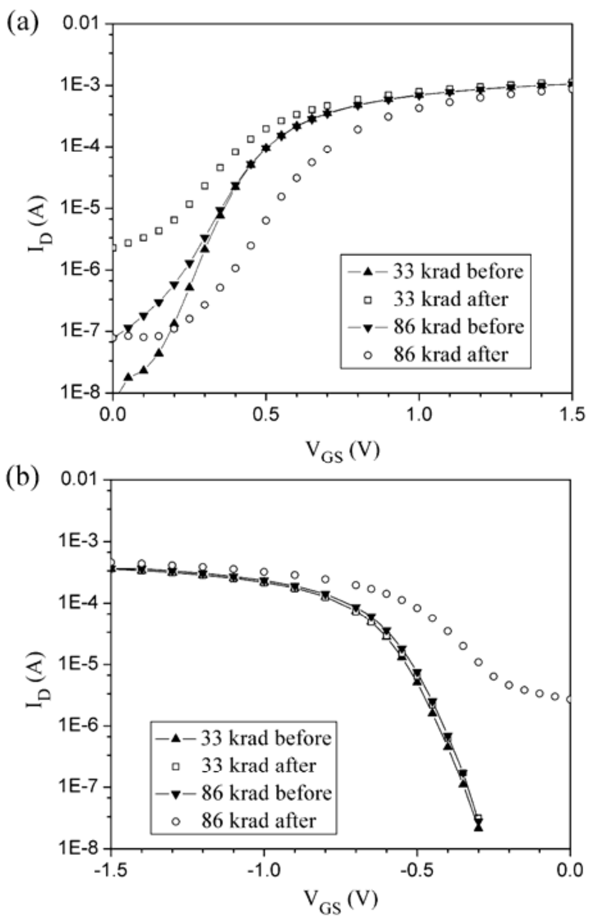


Fig. 2. The I-V curves of NMOS (a) and PMOS (b) ELT transistors before and after irradiation.

In general, the leakage current change can be attributed to radiation induced trapped charge and interface state. Our annealing study indicates that the interface state is not the major contribution to the leakage current change (see the annealing part later). The trapped change can be accumulations in three places: the gate oxide, the field oxide (edge) and the sapphire substrate (back channel). The ELT is able to eliminate effectively the edge leakage [9]. If the leakage current increase is due to the trapped charge in the gate oxide, the leakage current increase after irradiation comes from to the I-V curve shift. However, we moved the pre-irradiation ELT I-V curves by the threshold voltage shift caused by the irradiation (-0.08 V for NMOS at 33 krad(Si) and 0.18 V for PMOS at 86 krad(Si)). The corresponding current increases were very small in both NMOS and PMOS cases. Therefore, in the ELT most, if not all, of the leakage current increase comes from the back channel. This can be easily understood because the gate oxide is very thin (six nm) and the sapphire substrate is very thick (200 µm). Trapped positive charge in the sapphire causes leakage current in NMOS. Trapped negative charge in the back channel causes leakage current increase in PMOS. Since all NMOS and PMOS transistors share the sapphire substrate, the trapped charge's polarity in the back channel is a function of the total dose only and independent on the device type. The observations shown in Fig. 2 indicate that the net trapped charge in the sapphire is positive at low dose and becomes negative at high dose.

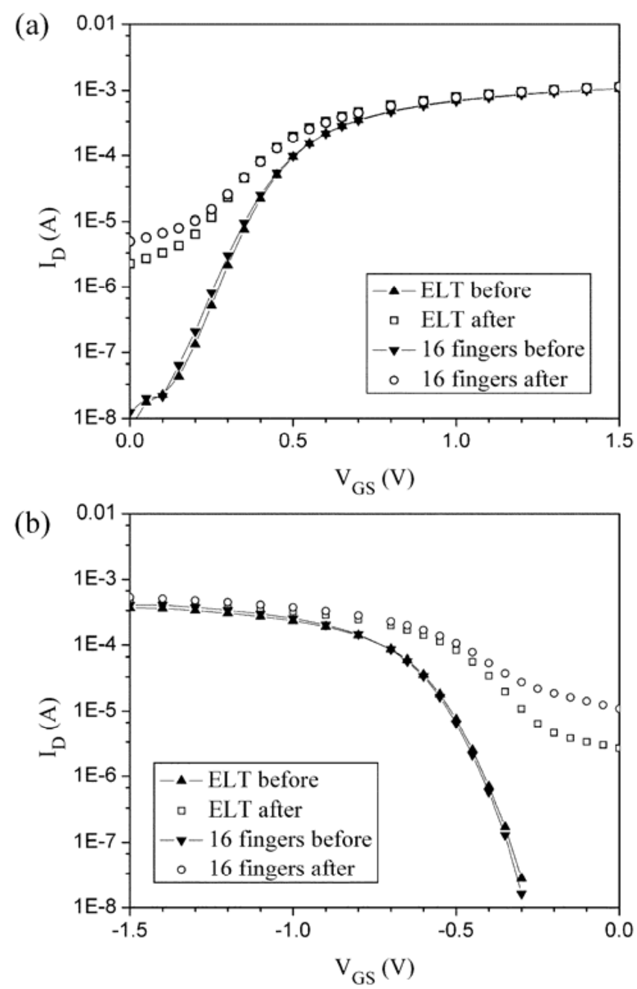


Fig. 3. The layout effect on NMOS (a) and PMOS (b) transistors.

In Fig. 3, we compare the I-V curves of the ELT and in standard transistors of 16 fingers at a dose with a large leakage current increase. The total dose is 33 krad(Si) for NMOS transistors and 86 krad(Si) for PMOS transistors respectively. The dose rate is 0.33 rad/s for both NMOS and PMOS transistors. All transistors have the same width of 40 µm and the same length of 0.25 µm. The leakage currents illustrated in the figure in the standard transistors are higher than those in the ELTs. The difference is the contribution from the radiation-induced edge leakage in the standard transistors. The fact that the edge leakage adds to the total leakage on top of the back channel indicates that the trapped charges in the field oxide and in the sapphire have the same sign. So in NMOS transistors, the net trapped charges in both the edge field oxide and in the sapphire are positive at low dose, causing parasitic conducting channels at the side (edge) of the gate and back of the transistor body. In PMOS transistors, the leakage current increase is only present at high dose when the net trapped charges in both the edge field oxide and in the sapphire become negative.

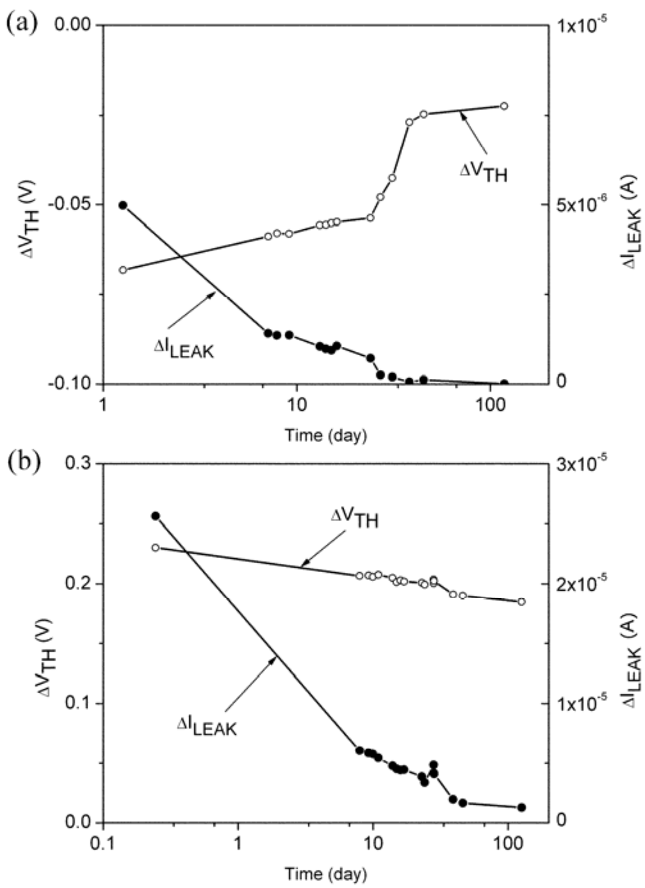


Fig. 4. The annealing studies of the NMOS (a) and PMOS (b) transistors.

As discussed in [3, 4], trapped holes are the main source of the trapped positive charges. These holes come from the radiation induced electron-hole pairs with the electrons diffused away. So leakage current increase in NMOS transistors, but not in PMOS, is reported in [3, 4]. In contrast, [13] suggests trapped negative charges in the sapphire substrate are produced by radiation, causing leakage current increase in PMOS transistors, but not in NMOS. We believe that these two processes compete and result in the polarity change in the net trapped charges with the total dose. With this, we explain that in NMOS transistors the leakage current rises when total dose is low, returns to pre-irradiated level when total dose is high; in PMOS transistors, the leakage stays unchanged when total dose is low, but rises when the total dose is high.

Shown in Fig. 4 are the annealing studies. Plotted are the leakage current increase (right vertical axis) and the threshold voltages shift (left vertical axis) compared to the pre-irradiation level. The horizontal axis is the time from the beginning of the irradiation. The transistors are W/L = 40 µm/0.25 µm in a 16-finger standard layout. The NMOS transistor is irradiated at 0.33 rad/s to a total dose of 33 krad(Si), the PMOS transistor at 8.3 rad/s to 100 krad(Si). As can be seen most of the increased leakage current anneals in 120 days. The annealing process is roughly linear with a logarithmic time axis, indicating that the dominating process follows the tunneling model discussed in reference [14]. The annealing process continues with time, indicating that the interface traps do not dominate the leakage current changes [15]. The threshold voltage shift is not large in NMOS and a big fraction of that anneals back. In the PMOS case this shift anneals from 0.23 V to 0.18 V in 120 days.

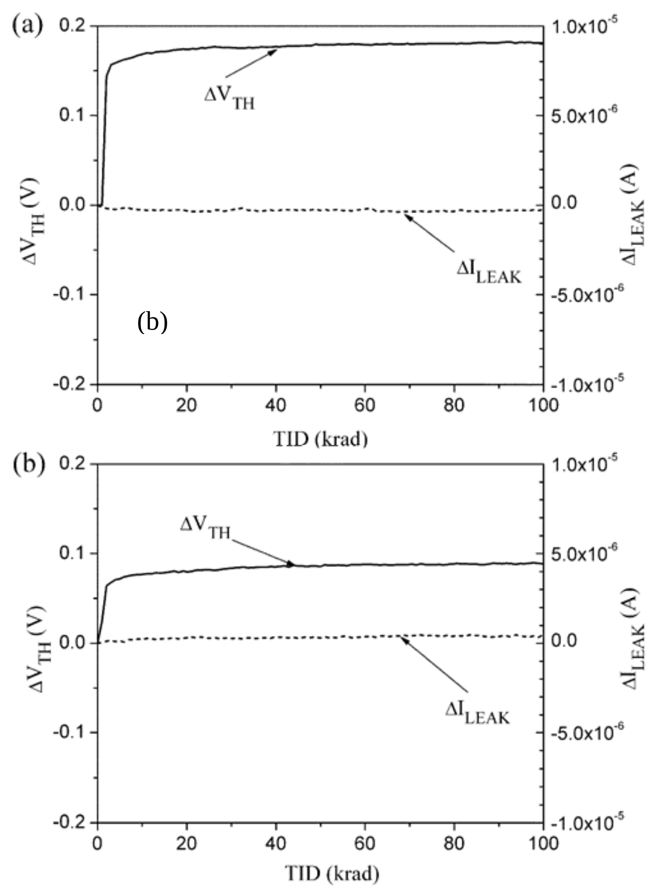


Fig. 5. NMOS (a) and PMOS (b) threshold voltage and leakage current change.

### B. *Sapphire substrate grounded*

A second TID measurement on the test chip is done with the sapphire substrate grounded during the irradiation. The results are shown in Fig. 5. All the transistors are 40 μm/0.25 μm in the 16-ginger standard layout. The dose rate is 0.33 rad/s. The leakage currents in both NMOS and PMOS are negligible throughout the irradiation. The threshold voltage shift quickly saturates with the total dose and stays unchanged through out the irradiation. These results show that grounding the substrate, which can be performed either at the package level or at the board level, can mitigate the TID effects in this SOS technology to negligible levels.

Electric potentials other than the ground level were also applied to the substrate during irradiation to provide more information about the mechanism that eliminates the buildup of trapped charges and hence eliminates the increase of leakage currents. More data analyses are also being carried out based on different transistor layouts to understand the effects in the edge channel and the back channel. The different reaction in threshold voltage and in leakage current with a grounded substrate also needs to be understood. We will present the results in the studies mentioned in this paragraph in a separated paper.

## IV. Studies on the Single Event Effects with 230 MeV Protons

An online test was done on the shifter registers and a logic latches in the chip with a 230 MeV proton beam. The proton fluence used in this test is $1.8\times10^{12}$ proton/cm$^2$ at the flux of $7.7\times10^{8}$ proton/cm$^2$/s. No error was reported before, during and after irradiation periods. The zero error result is translated into a cross section upper limit of $5.6\times10^{-13}$ cm$^2$ for all four tested units (standard layout shift registers, enclosed layout shift registers, resistively hardened shift registers, and latches). When comparing standard geometry based shift registers to enclosed geometry based shift registers, there was no difference in SEE immunity. In addition, since the standard geometry based shift register worked error free for the given radiation period, the resistively hardened technique showed no further benefit in relation to SEE immunity. The current consumption of these test elements was monitored during irradiation. Relating to the functionality of our test structures, there was no significant current change that inhibited device operation.

## V. Conclusion

A test chip with various test structures has been designed and fabricated in Peregrine's 0.25 μm Silicon-On-Sapphire CMOS UltraCMOS$^{TM}$ process technology and irradiated with a Co-60 gamma source and a 230 MeV proton beam. The sapphire substrate is left either floating or tied to ground when the transistors are irradiated with the Co-60 gamma irradiation up to 100 krad(Si). When the sapphire substrate is floating during irradiation, a radiation-induced leakage current increases in NMOS transistors at a low dose of 33 krad(Si) and in PMOS transistors at a high dose of 86 krad(Si). This is due to the net trapped charge polarity change with the increase of total dose. This leakage current increase anneals fast at room temperature and the annealing follows roughly the tunneling model. With the sapphire substrate grounded, the overall radiation-induced leakage current for both NMOS and PMOS transistors is negligible. The radiation-induced threshold voltage shift for both NMOS and PMOS transistors quickly saturates with the total dose and stays unchanged. SEE test with 230 MeV protons shows that this process has exhibited SEE immunity up to $1.8\times10^{12}$ proton/cm$^2$ fluence and within this fluence, there is no difference in SEE immunity among the four types of test structures. Our studies show that this technology is suitable for applications with total dose up to 100 krad and with a proton fluence up to $1.8\times10^{12}$ proton/cm$^2$.

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