Response of a 0.25 μm thin-film silicon-on-sapphire CMOS technology to total ionizing dose

2010 JINST 5 C11021

(http://iopscience.iop.org/1748-0221/5/11/C11021)

PUBLISHED BY IOP PUBLISHING FOR SISSA

RECEIVED: *October 13, 2010*
ACCEPTED: *October 25, 2010*
PUBLISHED: *November 29, 2010*

TOPICAL WORKSHOP ON ELECTRONICS FOR PARTICLE PHYSICS 2010,
20–24 SEPTEMBER 2010,
AACHEN, GERMANY

Response of a 0.25 μm thin-film silicon-on-sapphire CMOS technology to total ionizing dose

M.P. King,[a,1] **D. Gong,**[b] **C. Liu,**[b] **T. Liu,**[b] **A.C. Xiang,**[b] **J. Ye,**[b] **R.D. Schrimpf,**[a] **R.A. Reed,**[a] **M.L. Alles**[a] **and D.M. Fleetwood**[a]

[a] *Vanderbilt University,*
Nashville, TN 37235, U.S.A.
[b] *Southern Methodist University,*
Dallas, TX 75205, U.S.A.

E-mail: michael.p.king@vanderbilt.edu

ABSTRACT: The radiation response of a 0.25 μm silicon-on-sapphire CMOS technology is characterized at the transistor and circuit levels utilizing both standard and enclosed layout devices. The threshold-voltage shift is less than 170 mV and the leakage-current increase is less than 1 nA for individual standard-layout nMOSFET and pMOSFET devices at a total dose of 100 krad(SiO_2). The increase in power supply current at the circuit level was less than 5%, consistent with the small change in off-state transistor leakage current. The technology exhibits good characteristics for use in the electronics of the ATLAS experiment at the Large Hadron Collider.

KEYWORDS: Radiation damage to electronic components; Radiation-hard electronics

[1] Corresponding author.

doi:10.1088/1748-0221/5/11/C11021

Contents

2010 JINST 5 C11021

1 Introduction

Silicon-on-sapphire (SoS) complementary metal-oxide-semiconductor (CMOS) technology has been used in radiation-tolerant applications since the 1970s. SoS technologies exhibit several characteristics that make them attractive for use in radiation environments, including an insulating sapphire layer below the active silicon that eliminates the parasitic inter-device bipolar structure associated with latchup in bulk devices. SoS technologies also have been reported to have smaller single-event upset cross-sections than equivalent bulk processes [1]. However, radiation-induced leakage currents along the edges of the device and the back channel, where the active silicon meets the sapphire substrate, are important issues in these technologies [2]. The ATLAS experiment at the Large Hadron Collider is one example of an application for which SoS technology is very promising; the radiation environment is quite challenging compared to typical space and defense applications [3].

In this work, the radiation response of a 0.25 μm SoS CMOS technology is characterized at the transistor and circuit levels. Devices are evaluated in both standard and enclosed layout geometries. Radiation-induced charge trapping in the gate oxide results in threshold voltage shifts less than 170 mV for standard-layout transistors irradiated to a total dose of 100 krad(SiO_2). Additionally, increases in radiation-induced leakage current are less than 1 nA for standard-layout nMOSFET and pMOSFET devices. Circuit-level evaluation of these structures is consistent with these results.

2 Test structures and experimental conditions

The Peregrine 0.25 μm SoS process is a thin-film technology with both partially depleted and fully depleted devices. The epitaxial silicon layer is 80 nm thick with a 200 μm sapphire insulating substrate. The gate oxide thickness is 6 nm, and the process uses LOCOS for device isolation. Individual transistors and a set of shift registers were fabricated on a test chip.

Structures were fabricated in either standard or enclosed layout geometries. Three different transistor types were used with high, regular, or intrinsic threshold voltages. Devices with regular and high threshold voltages are partially depleted, while the intrinsic devices are fully depleted. Devices were packaged and subsequently baked for twelve hours at 150°C in preparation for irradiation. nMOSFET and pMOSFET irradiation bias conditions were V_D = 2.5 V and -2.5 V,

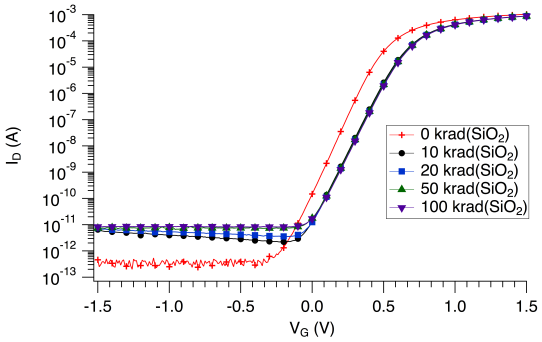

Figure 1. $I_D - V_G$ characteristics of an enclosed layout; regular threshold voltage nMOS SOS transistor.

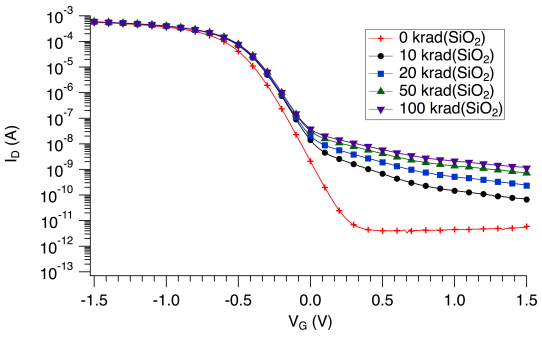

Figure 2. $I_D - V_G$ characteristics of an enclosed layout; regular threshold voltage pMOS SOS transistor.

respectively; all other terminals were grounded. This off-state condition is the worst case for inverters exposed to total ionizing dose [4]. The transistors were irradiated with 10 keV x-rays at a dose rate of 31.5 krad(SiO_2) per minute using an ARACOR Model 4100 irradiator. $I_D - V_G$ sweeps were performed to characterize the leakage current and threshold voltage of irradiated devices. Device characterization was performed with an HP 4156A parameter analyzer with an applied drain bias of ± 0.1 V for nMOS and pMOS transistors, respectively. Gate voltages were swept between -1.5 V and 1.5 V. The source and sapphire substrate were grounded during device characterization and irradiation.

Two types of shift registers, consisting of 32 D-flip-flop stages, one using standard layout transistors, the other enclosed layout transistors, were fabricated for circuit-level evaluation of radiation-induced leakage current. The power supply voltage for the shift registers was 2.5 V with the substrate grounded. The shift registers were irradiated with 198 MeV protons to a total fluence of 1.27×10^{13} cm^{-2} [5]. The operating frequency during irradiation was 40 MHz; the power supply current for each shift register was monitored with a Keithley 2700 multi-channel digital multimeter.

3 Experimental results

Typical pre- and post-irradiation $I_D - V_G$ characteristics are shown in figures 1 and 2 for nMOS and pMOS transistors. These devices are enclosed layout, regular threshold voltage devices, corresponding to $V_T = 0.55$ V and -0.35 V, for nMOS and pMOS transistors, respectively.

An initial positive shift in threshold voltage, with a maximum value of 170 mV, was observed at less than 1 krad(SiO_2) in both nMOSFET and pMOSFET devices, as seen in figure 3. This initial shift is due to radiation-induced electron trapping in the sapphire substrate [6]. These trapped electrons accumulate the back channel of nMOSFETs, and the front to back coupling results in a shift in threshold voltage. In pMOSFETs the trapped electrons couple the front and back gate similarly; however, they deplete the n-type body, leading to additional leakage current. No additional threshold-voltage shifts were observed following the initial exposure of 10 krad(SiO_2), up to the largest dose considered here (100 krad(SiO_2)).

2010 JINST 5 C11021

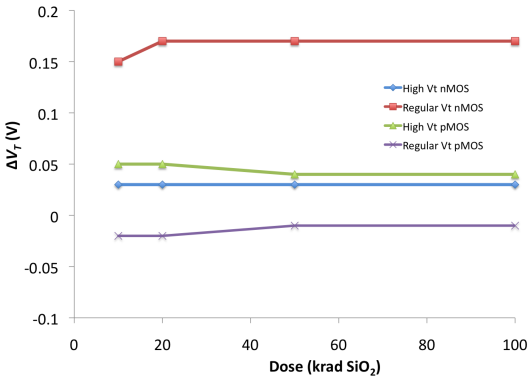

Figure 3. ΔV_T as a function of dose for partially depleted nMOS and pMOS devices.

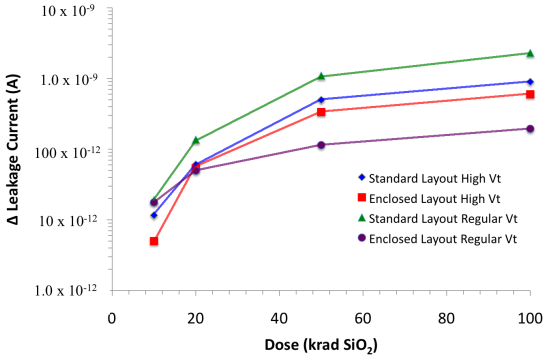

Figure 4. Change in leakage current with dose for high and regular threshold pMOSFETs with standard and enclosed layouts.

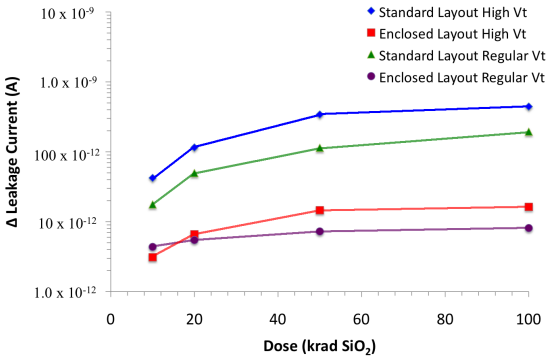

Figure 5. Change in leakage current with dose for high and regular threshold nMOSFETs with standard and enclosed layouts.

The radiation-induced leakage currents for standard and enclosed layout devices are shown in figures 4 and 5 for pMOSFETs and nMOSFETs, respectively. nMOS transistors in a standard layout configuration exhibit a parasitic conductive path along the edge of the device [7]. The enclosed layout transistors eliminate the edge leakage paths present in the standard layout nMOS devices. The edge leakage is associated with hole trapping in the isolation oxide, which affects nMOS transistors. Conversely, leakage paths exist for pMOS transistors primarily along the back channel of the device due to electron trapping, which impacts the threshold voltage of both nMOS and pMOS transistors. This back-channel leakage path exists and impacts both standard and enclosed layout device geometries.

The post-irradiation increase in power supply current at the circuit level is less than 5% (see figure 6), which is consistent with the relatively small radiation-induced change in off-state transistor leakage (less than 1 nA at 100krad(SiO_2) for both nMOSFET and pMOSFET devices). Leakage current was consistently higher for standard-layout devices than for enclosed-layout devices following irradiation because of the elimination of the parasitic edge leakage path in the enclosed-layout devices. The increase in circuit-level leakage current with increasing dose is caused by the formation of a back channel in the pMOS devices along the sapphire-silicon interface.

2010 JINST 5 C11021

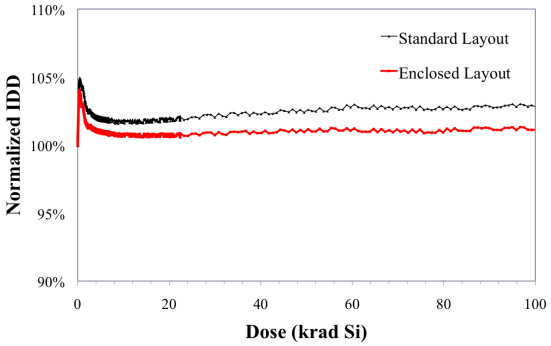

Figure 6. Normalized power supply current of standard and enclosed layout shift registers irradiated with 198 MeV protons.

4 Conclusions

Single transistors and shift registers fabricated in a 0.25 μm SoS CMOS technology were irradiated with 10 keV x-rays and 198 MeV protons, respectively. Radiation-induced electron trapping at the silicon-sapphire interface results in a shift in threshold voltage for both nMOS and pMOS transistors. The magnitude of the threshold-voltage shift was less than 170 mV, and saturated within 1 krad(SiO_2). At the transistor level, standard-layout pMOSFETs exhibited the largest increases in leakage current due to electron trapping at the back-channel interface. Radiation-induced leakage current was 1 nA or less for all device variants. This result is consistent with circuit-level results during proton irradiation of shift registers, and had little impact on circuit operation. These results indicate that this 0.25 μm SoS technology exhibits stable operating characteristics in a total dose environment of 100 krad(SiO_2), and appears to be very well suited for operating in the ATLAS TID environment.

Acknowledgments

The authors would like to thank Peregrine Semiconductor. This work is supported by US Department of Energy Grant DE-FG02-04ER41299.

References

[1] P.E. Dodd et al., *SEU-sensitive volumes in bulk and SOI SRAMs from first-principles calculations and experiments*, *IEEE Trans. Nucl. Sci.* **48** (2001) 1893.

[2] J.R. Srour et al., *Leakage current phenomena in irradiated SOS devices*, *IEEE Trans. Nucl. Sci.* **24** (1977) 2119.

[3] The Atlas Experiment, http://atlas.web.cern.ch/Atlas/GROUPS/FRONTEND/radhard.htm.

[4] V. Ferlet-Cavrois et al., *Worst-case bias during total dose irradiation of SOI transistors*, *IEEE Trans. Nucl. Sci.* **47** (2000) 2183.

[5] P. Paillet et al., *Comparison of charge yield in MOS devices for different radiation sources*, *IEEE Trans. Nucl. Sci.* **49** (2002) 2656.

2010 JINST 5 C11021

[6] R. Rios et al, *Radiation effects in fully-depleted CMOS/SOS*, *IEEE Int. SOI Conf. Proc.* (1991) 44.

[7] T.R. Oldham et al., *Post-irradiation effects in field-oxide isolation structures*, *IEEE Trans. Nucl. Sci.* **34** (1987) 1184.