Design and verification of a bit error rate tester in Altera FPGA for optical link developments

2010 JINST 5 C12003

(http://iopscience.iop.org/1748-0221/5/12/C12003)

PUBLISHED BY IOP PUBLISHING FOR SISSA

RECEIVED: *October 28, 2010*
ACCEPTED: *November 10, 2010*
PUBLISHED: *December 1, 2010*

TOPICAL WORKSHOP ON ELECTRONICS FOR PARTICLE PHYSICS 2010,
20–24 SEPTEMBER 2010,
AACHEN, GERMANY

Design and verification of a bit error rate tester in Altera FPGA for optical link developments

T. Cao, J. Chang, D. Gong, C. Liu, T. Liu, A. Xiang[1] and J. Ye

Southern Methodist University,
Dallas, Texas 75275, U.S.A.

E-mail: cxiang@smu.edu

ABSTRACT: This paper presents a custom bit error rate (BER) tester implementation in an Altera Stratix II GX signal integrity development kit. This BER tester deploys a parallel to serial pseudo random bit sequence (PRBS) generator, a bit and link status error detector and an error logging FIFO. The auto-correlation pattern enables receiver synchronization without specifying protocol at the physical layer. The error logging FIFO records both bit error data and link operation events. The tester's BER and data acquisition functions are utilized in a proton test of a 5 Gbps serializer. Experimental and data analysis results are discussed.

KEYWORDS: Optical detector readout concepts; Radiation-hard electronics; Front-end electronics for detector readout

[1]Corresponding author.

doi:10.1088/1748-0221/5/12/C12003

Contents

2010 JINST 5 C12003

1 Introducion

Multi-gigabit per second optical links are widely conceived to support data transmission in future particle physics experiments [1]. In order to qualify components and verify designs, link performance need to be evaluated in the laboratory and sometimes in a radiation environment. Bit error rate (BER) test is a fundamental measure of the integrity of each data transmission link, which traditionally requires expensive equipment with dedicated table-top testers. With the integration of high-speed transceivers inside a field-programmable gate array (FPGA), an embedded solution provides an economical alternative with the flexibility of customization to fit field radiation test scenarios.

We have developed a BER tester implemented in an Altera Stratix II GX signal integrity development kit [2]. The custom firmware is developed in VHDL and PC interface developed in LabVIEW. The tester features a pseudo random bit sequence (PRBS) generator and detector, as well as an error logging FIFO. The PRBS generator produces long stress patterns without using a lot of memory. The PRBS detector self-aligns to incoming bit streams without needing the receiver to acquire boundary alignment. Commercial BERT IPs [3] generally do not provide enough data acquisition capability for specified error analysis. In this tester, we implement an error logging FIFO to record both bit error data and link status. The throughput of a PC accessing the FIFO data is also optimized.

The tester's functionality is validated on an optical transmission test bench. BER vs. receiver sensitivity are measured to emulate stressed test conditions. The tester is also used in a proton test on custom serializer chips. Both bit flip and bit shift type of errors are recorded and analyzed.

2 Design

The custom bit error rate tester is an open source firmware and software package for high-speed serial pattern generation, error detection and data acquisition. It is implemented on the Altera Stratix II GX EP2SGX90 signal integrity development board. The tester operates up to 6.5 Gbps in 4

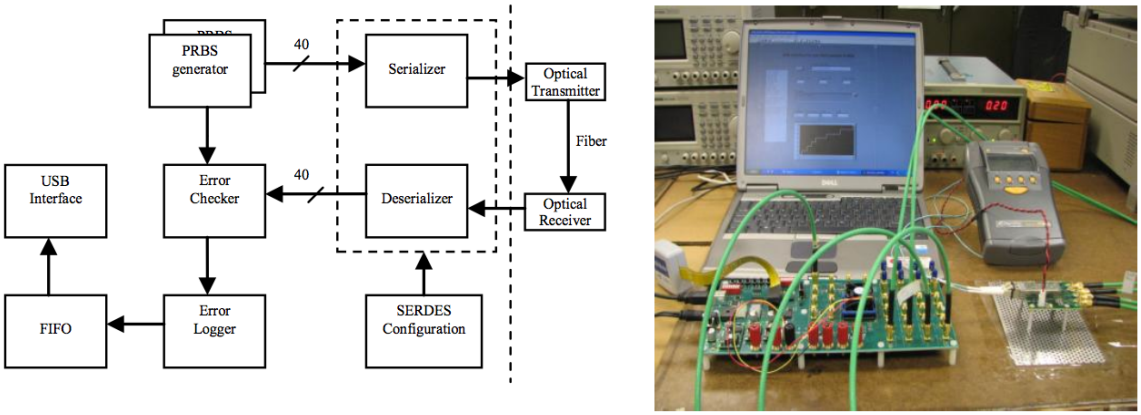

Figure 1. Block diagram of BER tester codes (left) and picture of BER tester setup (right).

duplex channels with analogue parameters, i.e., pre-emphasis, equalization, DC gain, and differential voltage adjustable during run-time. The tester comprises VHDL codes and LabVIEW routines. The main blocks of the VHDL codes are pattern generators, transceiver controls, error detector, link status monitor, and error logger, as shown in figure 1. The LabVIEW routines provide hardware control through periodic user interface refresh and acquire test data through USB to serial interface.

PRBS7, 23 and 31 patterns are generated using parallel to serial implementation. The internal data bus is 40 bit wide in order to match the speeds of parallel logic to serial transceiver circuitries. Given the auto-correlated nature of PRBS, word boundary is no longer checked. Upon start or reset, error detector first uses incoming data as seed to generate expected pattern, then switches to locked internal seed. Therefore once the link is stable, the incoming erroneous bit cannot disturb the error checking of the detector. Link locked signal is asserted when incoming data is error-free for a number of consecutive clocks and deserted when incoming data is erroneous for a number of consecutive clocks or when receiver clock is no longer valid. Link reset then can be initiated from transmitter or receiver individually, facilitating the test of separate components along a data link.

Five types of events are recorded in the error logging FIFO as shown in table 1. The recorded time stamp and the exclusive OR (XOR) pattern of the received and the expected data can reproduce transmitted data, given the pattern is a known PRBS. When a link-lost event occurs, it is logged in a reserved section of the FIFO. During the link lost event, bit error is not relevant and is no longer recorded. Instead the duration of the link-lost event is measured. The error logging FIFO is 12 bytes in width, matching the data type assignment. FIFO length is currently set to 4K each transceiver channel to balance the throughput and the dead time. The FIFO takes up 6% of available memory each single channel and 35% for the total 4 channels. Data acquisition efficiency is crucial in radiation test to minimize dead time during data collection. The tester sets USB in bulk mode [4] and achieves a throughput of 5 Mbps.

2010 JINST 5 C12003

Table 1. Error logging FIFO record types.

Event	Event flag	Time stamp	Event data	Note
SEE	001	48bit	XOR	
Locked	010	48bit	Expected data	Error detector locked to generator
Link lost	011	48bit	Expected data	Receiver CDR lost synchronization
FIFO Full	100	48bit	Expected data	Stop recording bit errors
FIFO Ready	101	48bit	Expected data	Resume recording bit errors

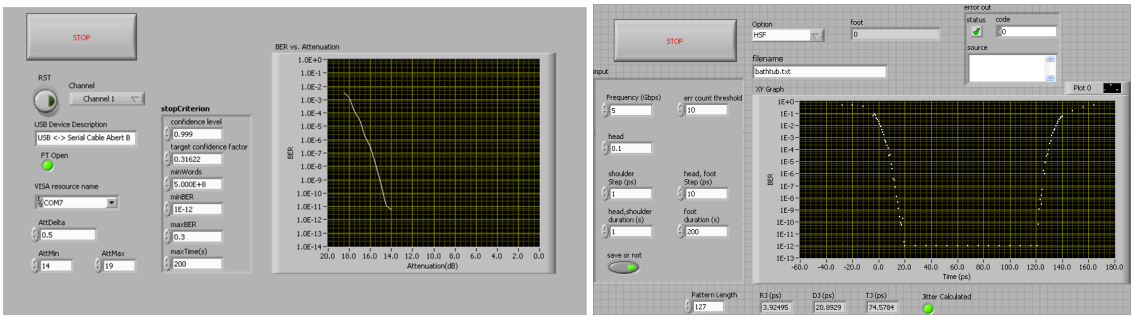

Figure 2. Custom BERT characterization routines. Left: BER vs. Optical power, right: transmitter BER scan curve, using a reference BERT receiver.

3 Test results

3.1 In lab verification

The BER tester is demonstrated on a point-to-point optical link as shown in figure 1. The tester's transmitter channel drives the transmitting side of an optical transceiver and the tester's receiver channel is connected to the receiving side of another optical transceiver. A variable optical attenuator is inserted in the fiber loop to stress the signal condition. In figure 2, we plot the optical attenuation versus the bit error rate in an automated LabVIEW routine. The relationship between the signal strength and BER can be used to determine the receiver sensitivity and to characterize the link power penalties. Receiver sensitivity of the same optical link is measured using the FPGA-based BER tester, a standalone BER tester, and the combination of the two. The differences are less than 1dB, comparable to measurement error floor. The data acquisition throughput of 5 Mbps is adequate even at a high error rate of 10^{-2}. FIFO access congestion happens when error detector is out of lock with pattern generator, but the receiver remains linked with incoming data stream, therefore the link lost signal remain deserted. The link can be reset from either transmitter or receiver side under this situation.

Figure 2 also demonstrates the characterization of the FPGA embedded transmitter. The measurement was taken from a transmitter channel of a Stratix II GX device feed into a standalone reference receiver, with error detection and sampling point shifting function. The resulted BER scan curve can be used to determine the precise total jitter and derive the random and deterministic jitter components. Jitter generation from the embedded transmitter mainly come from the VCO

2010 JINST 5 C12003

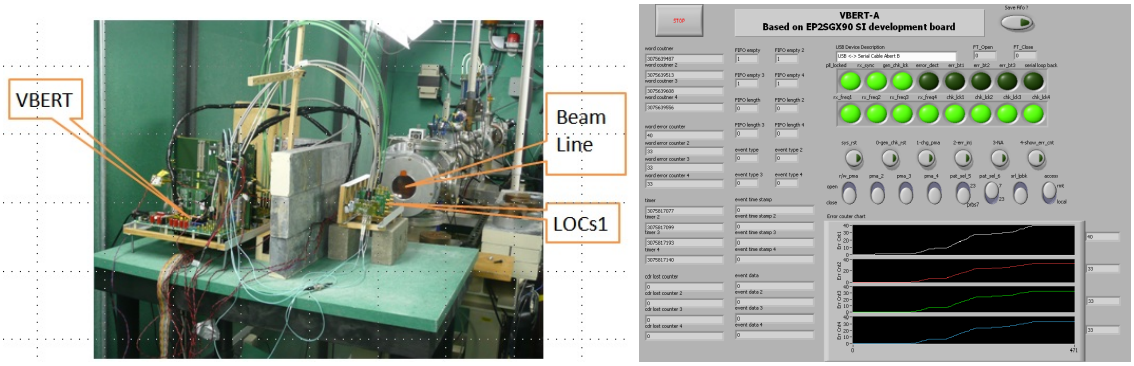

Figure 3. . Radiation test setup (left) and LabVIEW routine (right)

in the clock units. We measure the total jitter from the transmitter to be 0.26 UI at 5 Gbps. This qualifies the BER tester for providing electrical input interface to high speed optical links under development [5].

3.2 Radiation test application

We deployed the BER tester in a radiation test on a 5 Gbps custom serializer chip (the DUT) [6] with a 200 MeV proton beam at Indiana University Cyclotron Facility (IUCF). Parallel PRBS data generated from a Cyclone II FPGA were injected to the serilaizer chip carrier boards, and serialized data were then feedback to the BER tester receiver channels. The BER tester was placed in a shielded area behind lead bricks. Two serializer carrier boards were placed in the beam and another board in the shielded area as reference. The test setup is shown in figure 3. Front panel of the LabVIEW routine used to establish link connections and record error loggings is also shown in figure 3. The boards in the beam were put on adjustable axles to investigate the possible angle effect. The angles between the beam incident direction and die surface normal were changed from 0 to a maximum of 60 degree during the radiation test.

The beam flux stepped from low to high at various levels during a 12 hour run followed by a 15 hour annealing. No error was observed except at the highest flux level. When the flux reached the highest rate, a few errors occurred in both channels under radiation. We observed two types of single-event errors: single bit errors and synchronization errors. The single bit error events did not affect the link status afterwards, whereas the synchronization error required a receiver reset. With the two irradiated channels together, 5 single bit errors and 25 synchronization errors were observed. Taking the operating condition at the ATLAS liquid argon front-end crate in SLHC as an example, this upper limit of the error cross section translates to a proton induced bit error rate of 1.6×10^{-18}.

Post-test analysis of the error logging files shows that there are both 0 -1 and 1–0 transitions in the single bit errors, and that the synchronization errors result in exact one bit shift forward or backward, after a period of burst errors. The distribution of burst error lengths is shown in figure 4. The burst errors are heterogeneous yet constrained within two data frames, i.e., 80 bits of serial transmission. This suggests that a particle hit in the serializer circuitry can induce not only bit flips but also multiplexing errors or timing errors, and that the burst errors are likely to be confined.

2010 JINST 5 C12003

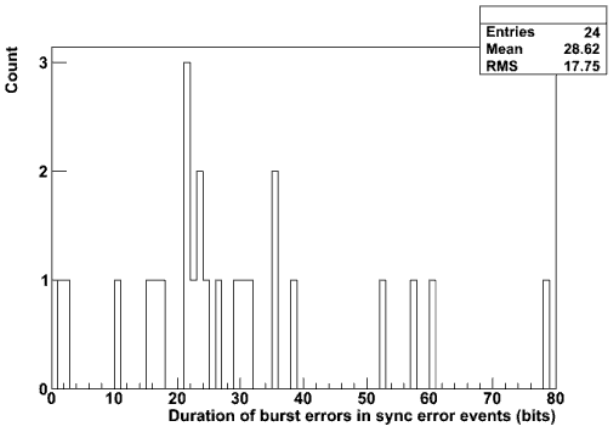

Figure 4. Distribution of burst error lengths of synchronization error events.

4 Conclusion

A customized bit error rate test bench using Altera's Stratix II GX transceiver development kit is demonstrated. The test bench implements PRBS generator and detector to produce long stress patterns and error logging FIFO to record both bit error data and link operation events. The test bench is used in a proton test on custom serializer chips where two types of SEE events are recorded. Besides single bit flip, the other type of error is analyzed and determined to be single bit shift.

Acknowledgments

The authors acknowledge US-ATLAS R&D program, and the US Department of Energy for funding this work. We would also like to thank Drs. Francois Vasey, Jan Troska and Paschalis Vichoudis at CERN, Alan Prosser and John Chramowicz at FNAL for beneficial discussions.

References

[1] F. Vasey et al., *The Versatile Link common project*, 2009 *JINST* **4** P12003.

[2] A. Xiang et al., *High-speed serial optical link test bench using FPGA with embedded transceivers*, in *Proceeding of the topical workshop on electronics in particle physics (TWEPP)*, Paris, France (2009).

[3] Altera, *Stratix II GX EP2SGX90 Transceiver Signal Integrity Development Board: Reference Manual*, online, http://altrea.com/literature/manual/rm_si_bd_2sgx90.pdf

[4] FTDI technical note, *FTDI USB data transfer efficiency*, online, http://ftdichip.com/Support/Documents/TechnicalNotes.htm.

[5] Fiber Channel Physics Interfaces, *FC-PI-5*, ANSI NCITs.352:2002

[6] D. Gong et al., *A 16:1 serializer ASIC for data transmission at 5 Gbps*, presented at the *Topical Workshop on Electronics for Particle Physics 2010*, 20–24 September 2010, Aachen, Germany.

2010 JINST 5 C12003